

Energy Efficient Memory Design using Low Voltage Complementary Metal Oxide Semiconductor on 28nm FPGA

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Abstract

In this work, we are designing a energy efficient memory circuit on 28nm FPGA. Four different LVC MOS are used to validate the energy efficient design. There is 40.67% power reduction when LVC MOS25 is used in place of LVC MOS33. LVC MOS25 is better than LVC MOS33 IO Standard according to our experiment. With LVC MOS15 there is 75.70% total power reduction in compare with the LVC MOS33. LVC MOS15 is most energy efficient IO Standard and LVC MOS33 is most power consuming IO Standard. To design a power efficient memory we are using Verilog as HDL, Xilinx ISE 14.6 simulator with kintex-7 FPGA.

Keywords: Energy Efficient, FPGA, IO Standard, Low Power, LVC MOS, Memory

1. Introduction

Role of IO standard is very crucial to make a power efficient digital circuit. IO standards are the input and output standards which are required to receive the input for the input receiver or to provide the result to output drive. In this work, we implemented our design on 28nm kintex-7 FPGA using Low Voltage Complementary Metal Oxide Semiconductor (LVC MOS) IO standard. Kintex-7 FPGA also supports different family of IO standard other than LVC MOS like SSTL, HSTL, and LVDCI. The core reason of this work is to explore a power optimized design to save the energy. Kintex-7 FPGA requires the low power and produces the high performance circuit. Kintex-7 28nm FPGA is a new class of FPGA which provides the 50% less power consumption than the previous 40nm devices.

LVC MOS is standard general purpose IO interface which provide a low voltage class of CMOS technology for unified impedance matching and to make a system to minimize the energy consumption in order to fulfill our goal of power optimized design of memory.

We implemented our logic on a memory chip. Random Access Memory (RAM) is a form of computer memory which is used to store the data. It allows the stored data to be accessed quickly in random order rather than sequentially. It is primary or main memory which is directly accessed by the CPU. It is used to read/write the data very quickly. It stores the data in form of pages inside it. There are different page replacement algorithms which can be used to replace the data of RAM (like FIFO and LRU) to optimize the search process. It is volatile memory and needs the power to keep the data accessible, if power is lost or off all data contained in memory will lose. SRAM and DRAM are the categorization of RAM. It can hold very few data at a time inside it and it is not a permanent storage device like a CD or hard drive.

In ¹ LVC MOS IO Standards have been studied on 3.3V and 1.8V for verifying the frequency. Result shows that, for Input Output Buffer (IOB) characterization a simple pass/fail test is sufficient. During Fault Injection (FI) those bits will shown that affect the voltage oscilloscope. Mitigation techniques are used to find out the incorrect

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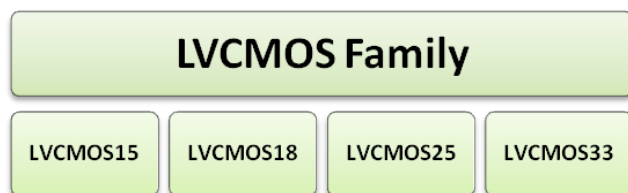


Figure 1. Family of LVCMOS IO Standard.

behavior of the bits. Triple Module Redundancy (TMR) is a most efficient and useful mitigation technique in which missing or incorrect behavior are triplicates and to implement this mitigation technique mitigation logic should be fabricated in advance in circuit. Basically the motive of this work is to evaluate the performance of output block when non-mitigated is compared with mitigated block of output.

In ² 0.5 μm SOI-CMOS is used with distributed RAM logic on LUT structure for designing and its verification. Here defined that pipeline design can be used to improve the hit ratio so that the output and address signal resisted synchronously. The design guarantees the improvement in frequency.

In ³ Integrated automatic optimization flow technique solves the problems of memory partitioning which is the combination of four techniques. This technique is user for memory optimization which is combination of memory partitioning and pipelining merged with data reuse to improve behavior synthesis.

In ⁴ Virtix-6 FPGA family of IO standards are used in ALU to reduce the power consumption and to design and implement a power efficient ALU. Power consumption will be increased when the frequency will increase because power is directly proportional with the frequency, so design of power efficient ALU directly depends upon the frequency passed in the circuit also. Family of LVCMOS is compared with three different families of IO standards like HSTL, SSTL, LVDCI and LVCMOS proved the most energy efficient IO standard for ALU among the rest.

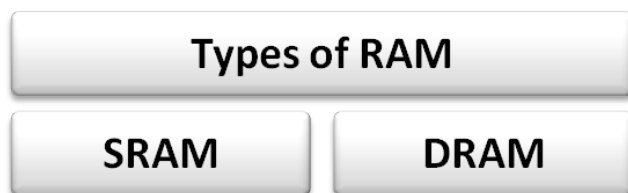


Figure 2. Random Access Memory (RAM) Categorization.

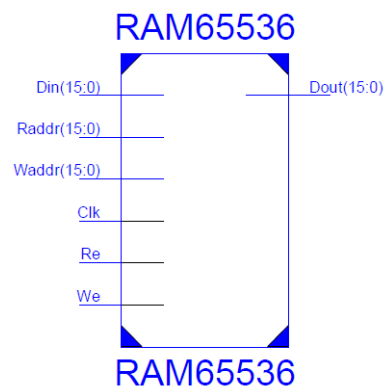


Figure 3. 16-bit RAM Implemented using Verilog HDL.

In ⁵, Low Voltage Digitally Controlled Impedance (LVDCI) is the family of IO standard used to find the best DCI to reduce the power consumption. LVDCI is used at 1.2V, 1.5V, 1.8V, 2.5V output drive and LVDCI_15 reduced 50percent of power consumption with comparison to other voltage in DCI. LVDCI_12 proved to most power efficient DCI and LVDCI_25 consumed the maximum power among the rest.

2. Block Diagram of Memory

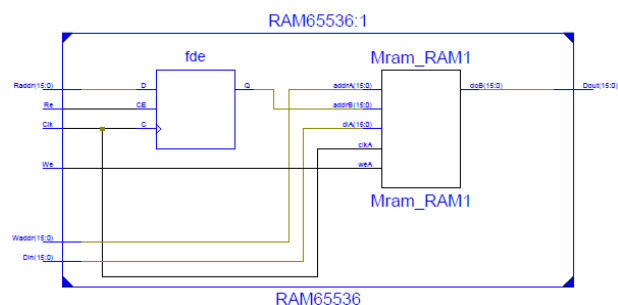
This is 16 bit RAM used in the experiment to design a power efficient circuit.

2.1 Top Level Schematic of 16-bit Memory

Read/Write capability is enabled in this RAM. The uniqueness of this design is that it is using a power efficient IO standard that makes it more energy efficient memory.

2.2 RTL Schematic of 16-bit Memory

RTL stands for Register Transfer Language. RTL schematic show how the logic is implemented and it is saved with *.ngr file extension. The term NGR means Native Generic Register File. In Figure 3, there are 16 data flip-flops.



3. Power Analysis

3.1 Power Consumption on 1 GHz

The categorizations of power are Static and Dynamic. Leakage power is static power and Clock, Logic, Signal and I/O powers are Dynamic Powers. In Table 1, Clock power remains 0.022W, Logic power remains 0.000W, Signal Power remains 0.026W and BRAMs Power remains 0.753W for LVC MOS IO Standard at voltage 1.5V, 1.8V, 2.5V and 3.3V with device operating on 1 GHz frequency. IO power get changed frequently when we change the voltage over LVC MOS.

Using Table 2 there is a 40.67percent power reduction when LVC MOS25 is used at place of LVC MOS33, 65.53percent power reduction when LVC MOS18 is used at place of LVC MOS33 to design the memory and 75.70percent total power reduction when LVC MOS15 is used at place of LVC MOS33 over 1GHz frequency.

Below in Figure 4, It shows the total power consumption between the LVC MOS family of IO standard at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operated over 1 GHz frequency.

This Figure 4 clearly shows that LVC MOS15 is most power saver IO standard and LVC MOS33 is consumes maximum power, So LVC MOS at voltage 1.5V is more Power efficient as compared to LVC MOS at voltage 1.8V, 2.5V and 3.3V on 1 GHz frequency.

Table 1. Power Consumption on 1 GHz Device Operating Frequency

	LVC MOS 15	LVC MOS 18	LVC MOS 25	LVC MOS 33
Clock	0.022 W	0.022 W	0.022 W	0.022 W
Logic	0.000 W	0.000 W	0.000 W	0.000 W
Signal	0.026 W	0.026 W	0.026 W	0.026 W
BRAMs	0.753 W	0.753 W	0.753 W	0.753 W
IOs	0.043 W	0.061 W	0.105 W	0.177 W
Leakage	0.082 W	0.082 W	0.083 W	0.084 W
Total	0.926 W	0.945 W	0.990 W	1.063 W

Table 2. Power Efficiency on 1 GHz in Comparison With LVC MOS33

	LVC MOS25	LVC MOS18	LVC MOS15
Reduction in Power (%)	40.67 %	65.53 %	75.70 %

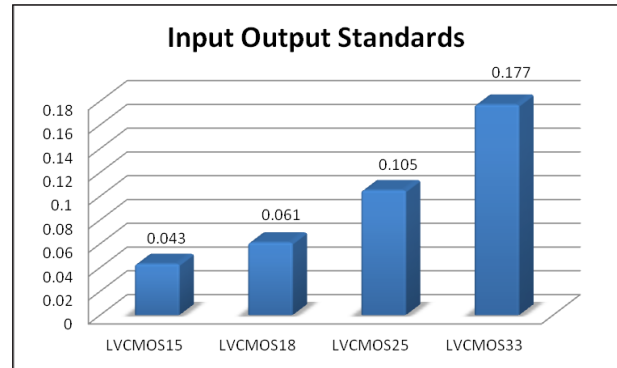


Figure 4. I/O Power Consumption on 1 GHz Device Operating Frequency.

3.2 Power Consumption on 10 GHz

In Table 3, Clock power remains 0.209W, Logic power remains 0.003W, Signal Power remains 0.224W and BRAMs Power remains 7.753W for LVC MOS IO Standard at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operating over 10 GHz frequency.

Table 4 shows, there is a 40.31 percent power reduction when LVC MOS25 is used by replacing LVC MOS33, 65.57 percent of power reduction when LVC MOS18 is used at place of LVC MOS33 and 75.93 percent total power reduction when LVC MOS15 is used at place of LVC MOS33 to design a power efficient memory over 10GHz frequency.

In Figure 5, that shows the total power consumption of the between the LVC MOS family of IO standard at

Table 3. Power Consumption on 10 GHz Device Operating Frequency

	LVC MOS 15	LVC MOS 18	LVC MOS 25	LVC MOS 33
Clock	0.209 W	0.209 W	0.209 W	0.209 W
Logic	0.003 W	0.003 W	0.003 W	0.003 W
Signal	0.224 W	0.224 W	0.224 W	0.224 W
BRAMs	7.535 W	7.535 W	7.535 W	7.535 W
IOs	0.425 W	0.608 W	1.054 W	1.766 W
Leakage	0.106 W	0.106 W	0.106 W	0.106 W
Total	8.531 W	8.685 W	9.134 W	9.850 W

Table 4. Power Efficiency on 10 GHz in comparison with LVC MOS33

	LVC MOS25	LVC MOS18	LVC MOS15
Reduction in Power (%)	40.31 %	65.57 %	75.93 %

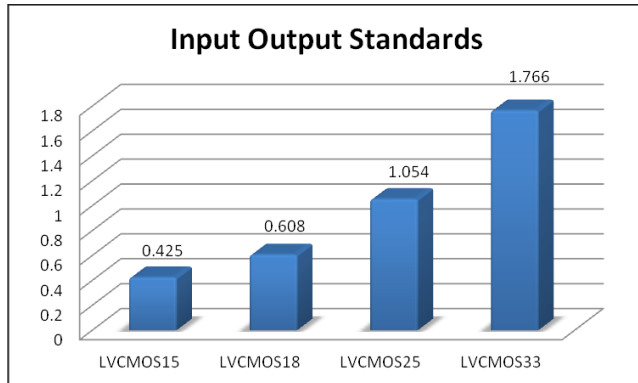


Figure 5. I/O Power Consumption on 10 GHz Device Operating Frequency.

voltage 1.5V, 1.8V, 2.5V and 3.3V on device operated on 10 GHz frequency. It clearly shows that LVCMOS at voltage 1.5V is most power efficient and LVCMOS33 is least power efficient family of LVCMOS IO standard when implemented to design a power efficient memory circuit, So LVCMOS at voltage 1.5V is more Power efficient as compared to LVCMOS at voltage 1.8V, 2.5V and 3.3V on 10 GHz frequency.

3.3 Power Consumption on 100 GHz

Table 5, shows the Clock power remains consistent at 2.110W, Logic power remains 0.010W, Signal Power remains 1.023W and BRAMs Power remains 75.346W for LVCMOS IO Standard at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operating on 100 GHz frequency.

Table 5. Power Consumption on 100 GHz Device Operating Frequency

	LVCMOS 15	LVCMOS 18	LVCMOS 25	LVCMOS 33
Clock	2.110 W	2.110 W	2.110 W	2.110 W
Logic	0.010 W	0.010 W	0.010 W	0.010 W
Signal	1.023 W	1.023 W	1.023 W	1.023 W
BRAMs	75.346 W	75.346 W	75.346 W	75.346 W
IOs	4.253 W	6.076 W	10.536 W	17.655 W
Leakage	1.050 W	1.050 W	1.051 W	1.052 W
Total	84.091 W	84.616 W	90.076 W	97.196 W

Table 6. Power Efficiency on 100 GHz in comparison with LVCMOS33

	LVCMOS25	LVCMOS18	LVCMOS15
Reduction in Power (%)	40.32 %	65.58 %	75.91 %

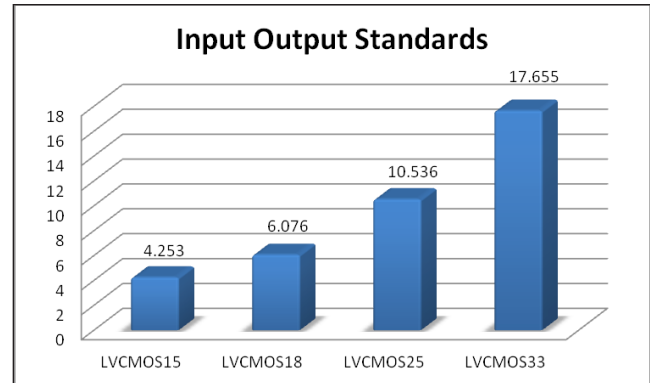


Figure 6. I/O Power Consumption on 100 GHz Device Operating Frequency.

In Table 6, there is a 40.32 percent power reduction when LVCMOS25 is used by replacing LVCMOS33, 65.58 percent of power reduction when LVCMOS18 is used at place of LVCMOS33 and 75.91 percent total power reduction when LVCMOS15 is used at place of LVCMOS33 to design a power efficient memory over 100 GHz frequency.

Figure 6, shows the total power consumption of the between the LVCMOS family of IO standard at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operated over 100 GHz frequency. It clearly shows that LVCMOS at voltage 1.5V is most power efficient and LVCMOS33 is least power saver family of LVCMOS IO standard, so LVCMOS at voltage 1.5V is more Power efficient as compared to LVCMOS at voltage 1.8V, 2.5V and 3.3V on 100 GHz frequency.

3.4 Power Consumption on 1 THz

Table 7, shows the Clock power remains consistent at 1.8W, 2.5V and 3.3V but it is 22.310W at voltage 1.5. Logic power remains 0.079W, Signal Power remains 8.985W at voltage 1.8V, 2.5V, and 3.3V and it fluctuate on voltage 1.5V. BRAMs Power remains 753.463W for LVCMOS at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operating on 1 THz frequency.

Table 7. Power Consumption on 1 THz Device Operating Frequency

	LVCMOS 15	LVCMOS 18	LVCMOS 25	LVCMOS 33
Clock	22.310 W	21.099 W	21.099 W	21.099 W
Logic	0.079 W	0.079 W	0.079 W	0.079 W
Signal	10.802 W	8.985 W	8.985 W	8.985 W
BRAMs	753.463 W	753.463 W	753.463 W	753.463 W
IOs	42.529 W	60.762 W	105.359 W	176.550 W
Leakage	1.050 W	1.050 W	1.050 W	1.050 W
Total	830.234 W	845.439 W	890.036 W	961.228 W

In Table 8, there is a 40.32 percent power reduction when LVC MOS25 is used by replacing LVC MOS33, This is same percentage of power reduction when the 100 GHz of frequency supplied to the circuit. It shows 65.60 percent of power reduction when LVC MOS18 is used at place of LVC MOS33 and 75.91 percent total power reduction when LVC MOS15 is used at place of LVC MOS33 to design a power efficient memory over 1 THz frequency.

Figure 7, shows the total power consumption between the LVC MOS family of IO standard at voltage 1.5V, 1.8V, 2.5V and 3.3V on device operated on 1 THz frequency. It clearly shows that LVC MOS at voltage 1.5V is most power efficient and LVC MOS33 is least power saver family of LVC MOS IO standard according to the Figure 7, So LVC MOS at voltage 1.5V is more Power efficient as compared to LVC MOS at voltage 1.8V, 2.5V and 3.3V on 1 THz frequency.

Our experiment to design a memory which consumes minimum power and gives the best result shows that, LVC MOS15 is the most and LVC MOS33 is least power efficient Low Voltage CMOS family of IO standard and there is slightly a minor change when we increase or decrease the frequency to the device. When we design and implement the memory circuit using LVC MOS IO standard at voltage 2.5V over 3.3V circuit the power reduction in percent is 40.67 percent at 1GHz, 40.31 percent at 10GHz,

Table 8. Power Efficiency on 100 GHz in comparison with LVC MOS33

	LVC MOS25	LVC MOS18	LVC MOS15
Reduction in Power (%)	40.32 %	65.60 %	75.91 %

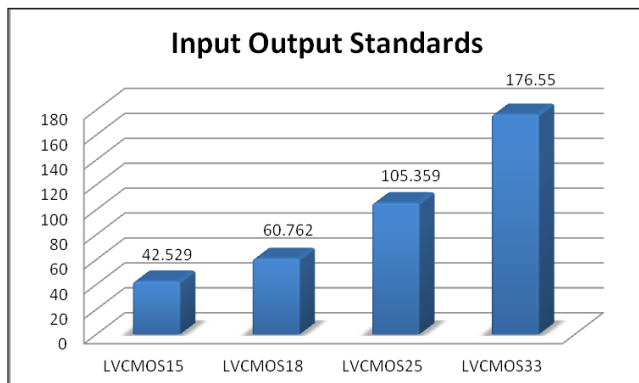


Figure 7. I/O Power Consumption on 1 THz Device Operating Frequency.

Table 9. Power Efficiency of LVC MOS family of IO Standards

	LVC MOS25	LVC MOS18	LVC MOS15
POWER REDUCTION	40.67% at 1 GHz	65.60% at 1THz	75.93% at 10 GHz

40.32 percent at 100 GHz and 40.32 percent at 1THz. So if we design memory using LVC MOS25, it will save maximum power at 1GHz frequency. Designing a circuit using LVC MOS18 over LVC MOS33 65.60 percent is maximum possible power reduction which is on 1THz frequency and when we use LVC MOS15 to design memory over LVC MOS33 there is 75.93percent total power reduction possible at 10 GHz frequency.

From the Table 9, it is clear that LVC MOS15 is the most power efficient when compared with LVC MOS33 and LVC MOS at voltage 3.3V is the least power efficient to design a power saver memory.

4. Conclusion

LVC MOS at voltage 1.5V is proved most power efficient IO standard and LVC MOS at voltage 3.3V is least power efficient among the 4 different Low Voltage Complementary Metal Oxide Semiconductor (LVC MOS) to design and implement a 16-bit power efficient memory circuit. LVC MOS15 reduces the power consumption of the circuit to 75.93% when it compared with the circuit which is designed using LVC MOS33 at Kentix-7 FPGA and the performance of LVC MOS15 is most power efficient at 10 GHz frequency.

5. Future Scopes

This design is implemented on 28nm Kentix-7 FPGA. There is a scope to redesign this memory on 16nm ultra scale FPGA in order to reduce the area on FPGA and minimize the power consumption of memory. We can also implement this design on Vertex FPGA at place of Kentix FPGA. In this work, IO standards are an effective technique to reduce the power consumption of a circuit. Therefore it is important to choose the correct IO standard to make a design which save the power and make it a power efficient circuit. IO standards can use in other devices also like Arithmetic and Logic Unit (ALU), Control Unit (CU), Memory Unit (MU) to increase their power efficiency.

6. References

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