

Comparative Analysis of Process Variation on Single Bit Domino Full Adder with Single Bit Static Full Adder

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Abstract

Testing and planning of very large scale integration circuits are the most challenging aspects now days, whenever a chip manufacture takes place many important parameters like doping of substrate, channel length of gate oxide and the thickness of the oxide vary during the fabrication of VLSI circuits that has an adverse impact on the circuit performance. In this paper, we demonstrate nearer examination of process variation on single bit domino full adder with single bit static full adder. This paper shows the variation of threshold voltage, oxide thickness and channel length on the execution parameter of single bit full adder that is designed by using a different transistor count like 10T, 28T, 22T. The result demonstrates that when 8.33% variation takes place in channel length than 2.078% increment in the power and 0.132% decrement in delay and 1.75% increase in power delay product of 22T domino full adder circuit, that is a minimum variation when compared with other single bit static full adders 10T and 28T. In threshold voltage when 1.6% variation occurs, then 0.76% decrement in power and 0.76% decrement in power delay product of 22 transistor domino full adder circuit, that is a minimum variation when compared with other single bit static full adder 10T and 28T. In oxide thickness 14.28% variation takes place, then 0.76% reduction in power and 2.49% decrement in PDP of 22T domino full adder circuit that is a minimum variation when compared with other single bit static full adder 28T and 10T. All simulations are done by using the tanner tool with 90nm PTM technology node with 1.1 volt supply voltage.

Keywords: Complementary Metal Oxide Semiconductor (CMOS), Metal Oxide Semiconductor (MOS), N-type Metal Oxide Semiconductor (NMOS), Power Delay Product (PDP), P-type Metal Oxide Semiconductor (PMOS), Threshold Voltage (VT), Very Large Scale Integration (VLSI)

1. Introduction

To fabricates any VLSI circuits is most challenging aspects, in spite of the fact that a special set of masks are used for the fabrication of integrated circuits, but yet after fabrication some VLSI chips exhibit longer delay times while some others exhibit shorter delay and also the output of the VLSI circuits vary as variation in device parameters that is caused by process fluctuations¹. Consequently, a critical parameter for design configuration is to reduce the effect of process variation on the performance of the circuit. The fabrication process of CMOS integrated circuits is highly

complex, even some minimum deviation is happening in mask alignment, implantation of some controlled amount of impurities, chemical etching of poly-silicon gate length of MOS transistors, and controlled thickness of the thin-gate oxide layer cannot be ignored.

The proper functioning of VLSI circuits mainly depends on the I-V characteristics of MOS transistors and the parasitic interconnections that can vary due to process variations. In this paper, we used the front end process variations, which refer to the changes at transistor level only. The prime component of the front end variant is transistor gate length, gate oxide thickness²

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and gate width, threshold voltage. These variations can cause drastic changes in the electrical parameters of the transistor that can lead to variations in the performance of the circuit².

$$I_d = \mu C_{ox} \frac{W}{L} f(V_{DS}, V_{GS}, V_T) \quad (1.1)$$

$$\tau_{PHL} = \frac{C_{load}}{K_n (V_{DD} - V_T)} \left[\frac{2V_T}{V_{DD} - V_T} + \ln \left(\frac{4(V_{DD} - V_T)}{V_{DD}} - 1 \right) \right] \quad (1.2)$$

The mobility (μ) of majority carriers in the substrate mainly depends on the level of dopants into it. The threshold voltage (V_T) is affected by the flat-band voltage of the MOS system, gate oxide capacitance (C_{ox}) is inversely proportional to the gate oxide layer thickness (t_{ox})³. This random fluctuation in this parameter will cause corresponding variations in the drain current that may be adversely affected into random variations in circuit performance such as power delay product, delay and power.

For designing a full adder there are two logic approaches first one is static style and the other one is dynamic style. A dynamic full adder is faster and more compact, required less silicon area, but it consumes more power and more sensitive to noise as compared to static full adder³.

The remaining of the paper is organized as follows: Section 2 shows the different single bit full adder that's designed by using static and domino logic design and Section 3 shows the result and discussion. In section 4 the paper is concluded.

2. 1-Bit Full Adder

2.1 28T Basic Static Full adder

The basic structure for any arithmetical circuit requires 28 transistors counts that designed by static logic approaches as shown in Figure 1. C, B, A is the inputs and Sum and Count are the output of static full adder³. In this adder circuit used 14 PMOS transistors and 14 NMOS transistors.

2.2 10T Static Full Adder

The second full adder implemented by using only 10 transistors through static logic approach. In this four-transistor XNOR module is used, as shown in the Figure 2. This module acts as a selector for two static multiplexers. But in this circuit XNOR signal has the V_{th} threshold loss problem that has effects on the output of the circuit⁴.

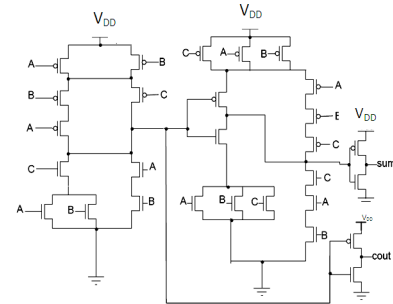


Figure 1. 28 transistor 1-bit full adder.

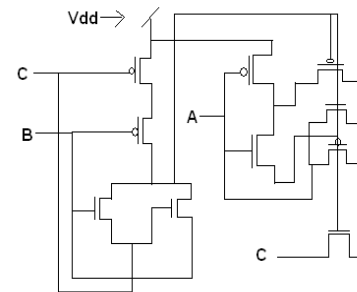


Figure 2. 10 transistor 1-bit full adder.

2.3 22T Domino Full Adder

The third full adder based on domino logic approach as shown in Figure 3. and implemented by using only 22 transistors count⁶. In this circuit between V_{dd} and GND there is no direct path and discharging of transistor depends on the clock signal. In this circuit when clock is 0 it's a precharging phase at this point dynamic node is charged up to VDD, when clock is 1 it's an evaluation phase, then, according to the input values A, B, C output of full adder evaluated in this phase.

In this paper, we used a transistor length $L_{min} = 90nm$ and Width W for all NMOS transistors is equal to L_{min} and for PMOS transistors is equal to $2L_{min}$ for designing the circuits. All the circuits optimized at 1.1 V supply voltage and 33 MHz input frequency conditions. To make good, reliable comparisons these conditions are kept same for all circuits.

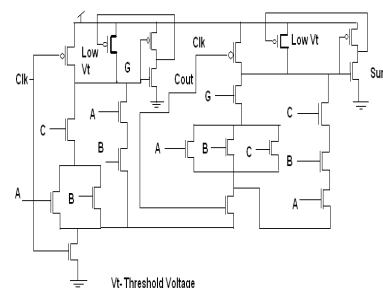


Figure 3. 22 transistor 1-bit full adder.

3. Results and Discussion

3.1 Impact of Threshold Voltage Variation on Power

In this analysis, we vary the threshold voltage (V_{th}) from 0.353 to 0.359 mV and note down the reading of power for different full adders. As per Table 1 and Figure 4, 22T domino full adder show minimum power dissipation, as we increase the threshold voltage it reduces the leakage current due to this leakage power of the circuit decreases and overall power of the circuit is also decreasing.

3.2 Impact of Threshold Voltage Variation on Delay

In this analysis, we vary the threshold voltage (V_{th}) from 0.353 to 0.359 mV and note down the reading of delay for different full adders. As per Table 2. and Figure 5., 22T domino full adder shows minimum delay. As we increase the threshold voltage it increases the drain current that leads to increase in the delay of the circuit as per from equation 1.2.

Table 1. Power vs threshold voltage

S. No	V_{th} Variation (mili Volt)	Power (μm)		
		28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	0.353	0.44162	1.951455	0.4122
2	0.354	0.40982	1.941782	0.41174
3	0.355	0.4056	1.932118	0.411276
4	0.356	0.39942	1.922461	0.410733
5	0.357	0.392447	1.912903	0.41007
6	0.358	0.38739	1.903243	0.40956
7	0.359	0.382733	1.893642	0.40904

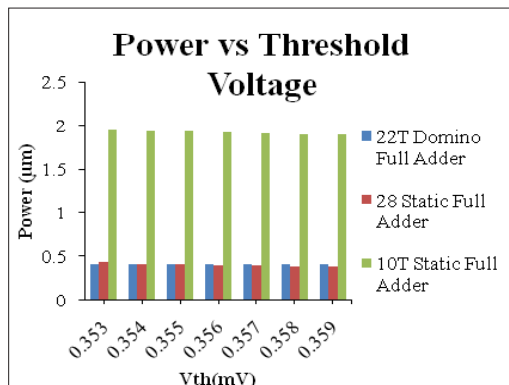


Figure 4. Variation of average power with threshold voltage for different adders

Table 2. Delay vs threshold voltage

S. No	V_{th} Variation (mili Volt)	Delay (ns)		
		28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	0.353	54.25	54.7	30.189
2	0.354	54.25	54.699	30.189
3	0.355	54.25	54.699	30.189
4	0.356	54.25	54.699	30.19
5	0.357	54.25	54.699	30.19
6	0.358	54.25	54.699	30.19
7	0.359	54.25	54.699	30.19

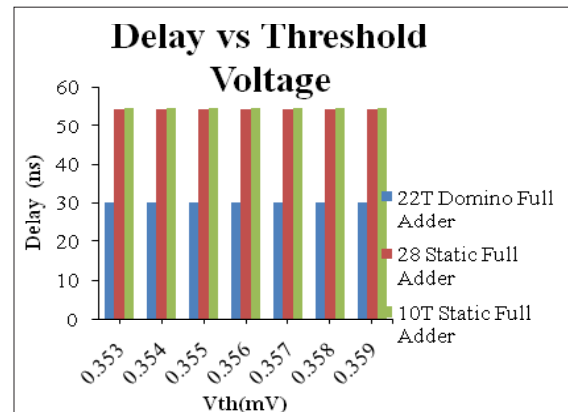


Figure 5. Variation of delay with threshold voltage for different adders.

3.3 Impact of Threshold Voltage Variation in Power Delay Product (PDP)

In this analysis, we vary the threshold voltage (V_{th}) from 0.353 to 0.359 mV and note down the reading of Power Delay Product (PDP) for different full adders. As per Table 3 and Figure 6. 22T domino full adder show minimum power delay product.

Table 3. PDP vs threshold voltage

S. No	V_{th} Variation (mili Volt)	PDP		
		28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	0.353	23.95789	106.7446	12.44391
2	0.354	22.23274	106.2135	12.43002
3	0.355	22.0038	105.6849	12.41601
4	0.356	21.66854	105.1567	12.40003
5	0.357	21.29025	104.6339	12.38001
6	0.358	21.01591	104.1055	12.36462
7	0.359	20.76327	103.5803	12.34892

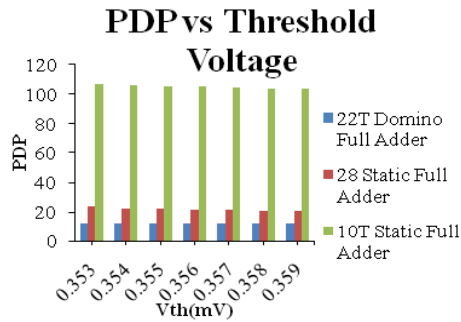


Figure 6. Variation of PDP with threshold voltage for different adders.

3.4 Impact of Oxide Thickness Variation on Power

In this analysis, we vary the oxide thickness (t_{ox}) from 1.2 nm to 1.8 nm and note down the reading of power for different full adders. As per Table 4 and Figure 7, 22T domino full adder show minimum power dissipation as compared to the other static full adders. As we increase the oxide thickness it reduces the oxide capacitance that decreases the drain current as per from equation 1.1 therefore power dissipation decreases.

Table 4. POWER Vs OXIDE THICKNESS

S. No	Power(μ m)			
	Oxide thickness (t_{ox} nm)	28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	1.2	1.165	0.81438	0.49752
2	1.3	1.11102	0.81062	0.49402
3	1.4	1.0486	0.78278	0.48984
4	1.5	0.99871	0.75805	0.48379
5	1.6	0.95794	0.734507	0.47751
6	1.7	0.92037	0.71352	0.47158
7	1.8	0.89927	0.69935	0.46659

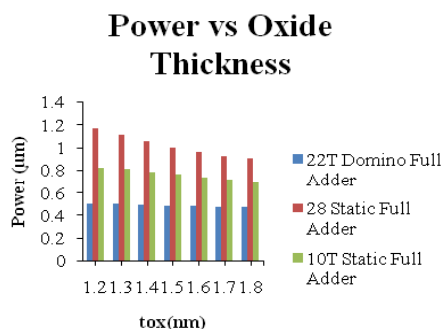


Figure 7. Variation of Power with Oxide thickness for different adders

Table 5. Delay vs Oxide Thickness

S. No	Oxide thickness (t_{ox} nm)	Delay(ns)		
		28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	1.2	54.248	54.787	30.167
2	1.3	54.248	54.793	30.17
3	1.4	54.248	54.799	30.173
4	1.5	54.249	54.806	30.176
5	1.6	54.249	54.812	30.179
6	1.7	54.249	54.819	30.182
7	1.8	54.249	54.825	30.185

Delay vs Oxide Thickness

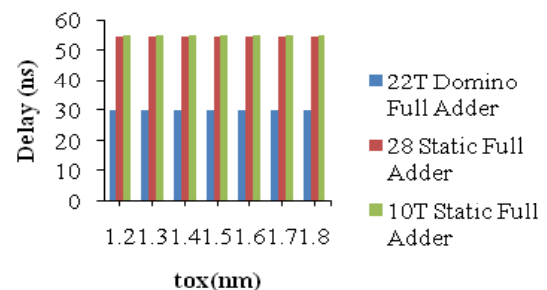


Figure 8. Variation of Delay with Oxide thickness for different adders

3.5 Impact of Oxide Thickness Variation on Delay

In this analysis, we vary the oxide thickness (t_{ox}) from 1.2 to 1.8 nm and note down the reading of delay for different full adders. As per Table 5 and Figure 8, 22T domino full adder shows minimum delay as compared to the other full adders. As we increase the oxide thickness it reduces the oxide capacitance that decreases the drain current as per from equation 1.1 therefore delay of the circuit increases.

3.6 Impact of Oxide Thickness on Power Delay Product (PDP)

In this analysis, we vary the oxide thickness (t_{ox}) from 1.2 to 1.8 nm and note down the reading of power delay product for different full adders. As per Table 6 and Figure 9, 22T domino full adder shows the minimum power delay product as compared to the other full adders corresponding to oxide thickness variation.

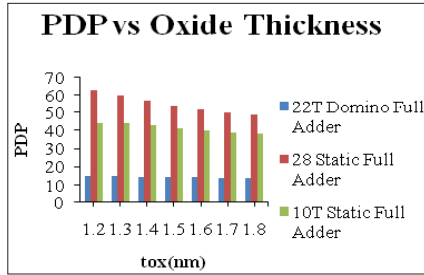


Figure 9. Variation of Power Delay Product with Oxide thickness for different adders

3.7 Impact of Effective Length on Power

In this analysis, effective length (L_{eff}) varied from 7.2 to 7.9 nm and the reading of power for different full adders was recorded. As per Table 7 and Figure 10, 22T domino full adder shows minimum power dissipation as compared to other full adders. Generally the effective length of the inverter is $L' = L - \Delta L$ where ΔL is the marked length that separates the pinch-off point from the drain edge. This marked length is represented in the model file by using lint notation. As we increase the effective length that decreases the threshold voltage due to this leakage current of the circuit increases, which results in increase the power dissipation of the circuit.

Table 7. Power vs Effective Length

S. No	Power(μm)			
	Effective Length (lint nm)	28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	7.2	0.825907	0.5928276	0.446446
2	7.3	0.834023	0.6014805	0.447466
3	7.4	0.842252	0.6145615	0.451176
4	7.5	0.850606	0.6258894	0.452274
5	7.6	0.859256	0.6376326	0.454729
6	7.7	0.868024	0.649885	0.454658
7	7.8	0.876973	0.6623294	0.455724
8	7.9	0.886173	0.6746208	0.45434

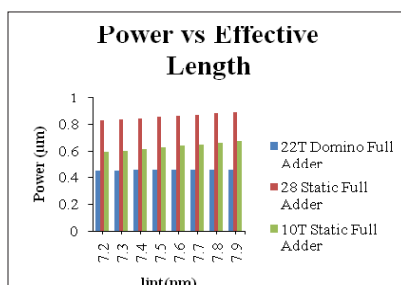


Figure 10. Variation of Power with Effective Length for different adders

Table 8. Delay vs Effective Length

S. No	Delay(ns)			
	Effective Length (lint nm)	28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	7.2	54.249	54.811	30.182
2	7.3	54.249	54.809	30.182
3	7.4	54.248	54.808	30.181
4	7.5	54.247	54.807	30.181
5	7.6	54.246	54.805	30.18
6	7.7	54.244	54.804	30.18
7	7.8	54.243	54.802	30.179
8	7.9	54.242	54.801	30.178

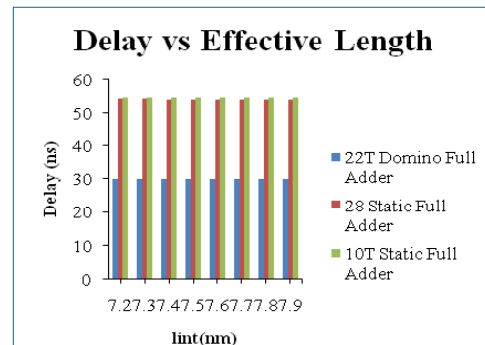


Figure 11. Variation of Delay with Effective Length for different adders

3.8 Impact of Effective Length on Delay

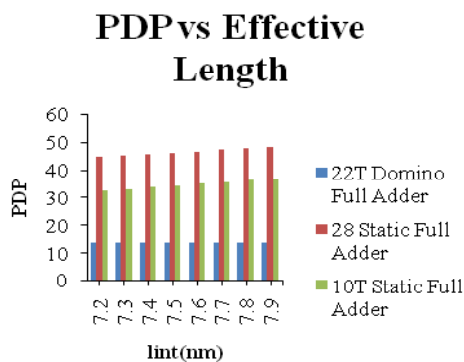
In this analysis, we vary the effective length (L_{eff}) from 7.2 to 7.9 nm and note down the reading of delay for different full adders. As per Table 8 and Figure 11, 22T domino full adder shows minimum delay as compared to other full adders. As we increase the effective length that decreases the threshold voltage corresponding to that drain current of the circuit decreases that result in decreases in delay of the circuit as per from equation 1.2

3.9 Impact Of Effective Length on Power Delay Product (PDP)

In this analysis, we vary the effective length (L_{eff}) from 7.2 to 7.9 nm and note down the reading of power delay product for different full adders. As per Table 9 and Figure 12, 22T domino full adder shows the minimum power delay product as compared to other full adders. As we increase the effective length it overall increases the power delay product of the circuit.

Table 9. PDP Vs Effective Length

S. No	Effective Length(lint nm)	PDP		
		28T Static Full Adder	10T Static Full Adder	22T Domino Full Adder
1	7.2	44.80462	32.49347	13.47463
2	7.3	45.24494	32.96654	13.50542
3	7.4	45.69051	33.68289	13.61695
4	7.5	46.14283	34.30312	13.65008
5	7.6	46.61122	34.94545	13.72372
6	7.7	47.08507	35.6163	13.72157
7	7.8	47.56966	36.29698	13.7533
8	7.9	48.06782	36.96989	13.71106

**Figure 12.** Variation of PDP with Effective Length for different adders

4. Conclusion

We have studied show how the variations of process parameter affect the performance parameter, i.e power delay product, delay and power consumption of different full adder circuits. These are the important parameters which taken into consideration while fabricating any VLSI circuits. But if we compare the overall effect of variation of process parameter, i.e. threshold voltage, channel length and thickness oxide, it was minimum in domino full adder using 22 transistor count and maximum in static full adder containing 10 transistor count. In threshold voltage 1.6% variation occurs, then 0.763% decrease in PDP and 0.76% decrease in power of 22T domino full adder as compared 15.38% decrease in PDP and 13.33% decrease in power of 28T static full adder and 2.965 decreases in delay and 2.96% decrease in power of 10T static full adder. In effective length 8.33% variation occurs, then 0.13% reduction in delay and 1.75% increase in PDP and 2.07% increase in power of 22T domino full adder as compared 0.01% reduction in delay and

7.28% increase in PDP and 6.18% increase in power of 28T static full adder and 11.72% increase in power and 0.018% reduction in delay and 13.77% increase in PDP of 10T static full adder. In oxide thickness 14.28% variation occurs, then 2.49% reduction in delay and 2.517% decrease in power of 22T domino full adder as compared to 8.644% decrease in PDP and 8.64% decrease in power of 28T static full adder and 6.14% reduction in PDP and 6.16% decrease in power of 10T static full adder. In future we extend this work to study how with in die variations affect the power consumption, delay and power delay product of any VLSI circuits.

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