

Design and Analysis of High Gain, Low Power and Low Voltage a-Si TFT based Operational Amplifier

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Abstract

This paper investigates on the design of two stage Operational Amplifier (Op-Amp) with NMOS input at differential stage. This low power Op-Amp designed with Amorphous Silicon Thin Film Transistor (a-Si TFT) and MOS transistor. It is observed that the newly designed TFT Op-AMP operates in low voltage at 3V DC, with high gain, high output impedance and high phase margin and moderate power dissipation. A detailed design procedure is carried-out to design the proposed Op-Amp. HSPICE Circuit Simulator is used for simulation. Obtained results are compared with CMOS Op-Amp which uses the same circuit and design procedure. The output behavior of TFT Op-Amp is also compared with the existing work showing good agreement.

Keywords: Amorphous Silicon, CMOS, High Stability, Low Power, Operational Amplifier, Thin Film Transistor

1. Introduction

Thin-film transistors have undergone extensive evolution, development and refinement, since their conception in the modern electronic world. As their intended uses went from switching systems to low cost computer logic to flat panel display addressing new materials, structures and fabrication techniques were introduced. Amorphous Silicon (a-Si) is most widely used active layer material while Poly-Si is increasingly pursued as a next generation TFT technology. Thin-film transistors are from Insulated Gate FET family. TFT differs from a typical MOSFET in that it is composed of very thin layer deposited on an insulating substrate, whereas most MOSFETs are formed from a semiconductor wafer. TFTs are gaining more interest in large area electronics such as flexible displays, RFIDs, sensors, switching systems, solar cells, RAMs, low cost computer logic, flat panel for image crystallization etc., They draw more attention towards the application of different types of TFTs. Mainly a-Si, and Poly-Si, increases

need for an accurate and efficient material to simulate the circuits used on these devices.

This paper is organized into the following sections. The Section 2, introduces the structures and modeling aspects of thin film transistor. Section 3, dealt about the TFT Operational Amplifier circuit. Detailed design procedure of TFT based Op-Amps and their analysis are discussed in section 4. Finally in section 5, the result has been discussed and concluded.

2. Thin Film Transistors

Polycrystalline Silicon (Poly-Si) Thin Film Transistor (TFT) technology is critically important for large area electronics, especially for flat panel active matrix liquid crystal display applications and for high density static random access memory circuits¹. In particular, various research works have been carried out on low temperature Poly-Si TFTs because they can be used for integrating driving circuits and pixel elements on a common

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substrate in flat panel displays. The reason behind is that Poly-Si TFTs have much higher electron mobility and drive current compared with a-Si TFTs^{2,3}. However, these advantages could not be fully realized in the early days of Poly-Si TFT technology. Because of Solid Phase Crystallization process was the only source of acquiring the Poly-Si films. Due to low-temperature processes that have to be used for glass substrates, numerous defects in Poly-Si grains and at grain boundaries were exist and degraded the device characteristics. In recent years, these issues have been mainly overcome by using a variety of advanced crystallization processes that have been developed and explained^{2,4}. Fabrication of Poly-Si TFT is possible and can be utilized for various research work and implementation.

Due to its low temperature process, Poly-Si TFT has become essential device both in low cost Integrated Circuits and in microelectronics. An abnormal leakage current is the main deficiency of Poly-Si TFT and present inconsistently in the device. This current is depending strongly on the bias and temperature which has been generated from grain boundary defects near the drain. The main reason of the abnormal leakage current is due to the field assisted generation mechanism.

Figure 1 shows the structure of Poly-Si TFT is a three terminal device. The substrate of Poly-Si TFT is floating just like SOI MOSFET. The modelling of Poly-Si TFT is the effective medium of approach which treats the non-uniform Poly-Si sample with grain boundaries as some uniform effective medium with effective material properties. The increase of drain current in saturation is caused by the floating body effect. This

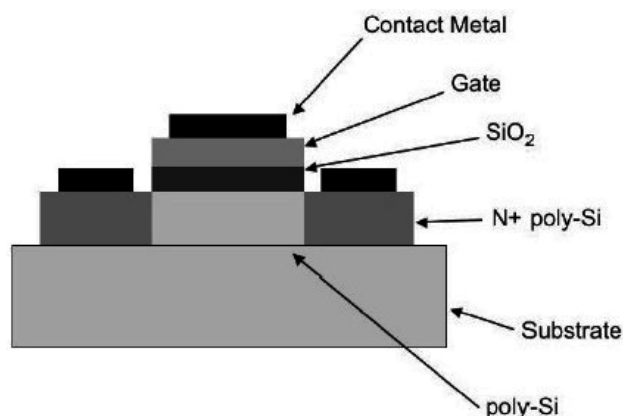


Figure 1. Poly-Si structure with different layers.

short channel devices show a significant decrease of the sub-threshold ideal factor with increasing drain voltage. By using this model, the relations of leakage current between terminal voltages, temperature of the TFT can be obtained.

The bottom gate structure of a-Si:H TFT is shown in Figure 2, which is also a three terminal device. The operation of a-Si TFT is quite different from that of crystalline MOSFET. In the sub-threshold region the drain current is a poor function of the gate voltage dictated by large trap density in the material in case of crystalline MOSFETs. Above threshold most of the induced charge in a-Si:H TFT goes into traps and only a small fraction enters the conduction band. This fraction increases as the gate voltage increases. The field effect mobility increases with the gate voltage.

The simplest Organic TFT models are very similar to those for conventional p-channel MOSFETs. The field effect mobility might depend on the channel length and transport properties are very sensitive to the properties of organic semiconductor gate di-electric interface. In the structure of organic p-channel TFTs uses Pentacene as the active layer. Aluminum acts as the gate metal and Parylene as the gate dielectric⁵. Finally, the devices are encapsulated using a Parylene process. D.A Johns and K. Martin highlighted the fact that the saturation mobility is 0.08 with an on/off current ratio greater than ZnO⁷ and recently, ZnO (and its derivatives) has attracted interest due to its higher mobility and electrical stability^{6,8,9}. In our research work, we have concentrated on Poly-Si and a-Si TFTs to be used in the Op-Amp.

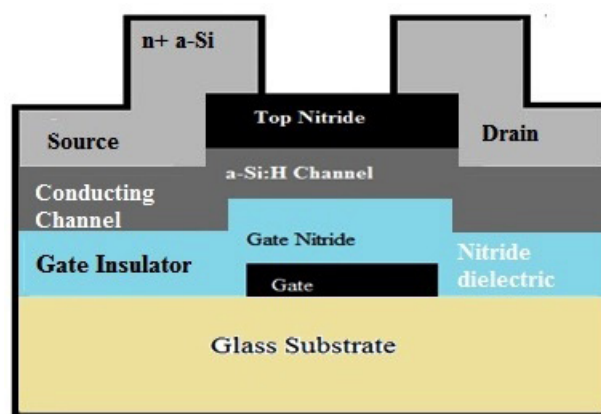


Figure 2. Bottom gate structure of an a-Si:H TFT.

3. TFT based Operational Amplifier

3.1 Related Work

An Op-Amp is the core component of surprisingly larger application in modern electronic era and undoubtedly one of the most useful mixed signal circuitry. An Op-Amp is usually, a single-ended output with a differential input of an electronic voltage amplifier of high gain. Its differential input is either NMOS input or PMOS input.

Op-Amp, which was first, realized in vacuum tubes manifestos in the 1950s. The first semiconductor engineering was introduced with integrated circuit used with Op-Amp in 1964, which is used in most analog and mixed signal ICs¹⁰. Op-Amp is the key component in analog processing systems¹⁷. The demand for mixed signal ICs are considerably increasing, which makes more critical to the Op-Amp design.

The main challenges of Op-Amp are a high dc gain and a high bandwidth with a high output swing depending on the applications. To achieve a higher gain, multi-stage Op-Amp can be used by cascading the stages¹¹. If the gain is increased the bandwidth will be considerably reduced, which is the drawback of the two stage Op-Amp. However, it is difficult to compensate and hard to stabilize for the two-stage Op-Amp, which is widely used in many applications¹².

Frequency compensation technique is necessary to avoid closed loop instability. The easiest method for compensation is to connect a capacitor between input and output of the second stage¹⁰. This method gives high closed loop stability with lower bandwidth and results in splitting the poles. The Cascade compensation technique has been introduced to improve the stability performance¹³. This technique improves the settling performance and the output swing is limited to certain range¹⁴. Single Miller Feed Forward Compensation technique is proposed and this technique improves stability and attenuates the bandwidth reduction¹⁵. However, this method suffers from compressed gain bandwidth problem because of very high gain of the first stage¹⁶.

3.2 Op-Amp using TFT

TFTs operate on low power voltage and low static power consumption like MOSFET and CMOS, but they are highly immunity to noise. When TFT device is switching between on and off states, it is drawn only a significant

power. Also, they are not producing much heat as MOSFETs. These TFT devices also allow a high density of logic functions on a chip.

In our previous work¹⁸⁻²², we designed an Op-Amp using a-Si TFT and Poly-Si TFT. Also, we discussed about the design constraints and finally approached to the well-designed Op-Amp and explained that reason for using two types of TFT devices such as amorphous Si TFT and Poly-Si TFT. We proposed a two stage a-Si TFT based Op-Amp circuit which is shown in Figure 3. Simulations are carried out on the design of a-Si TFT as well as CMOS based Op-Amps. In a-Si TFT based Op-Amp, a-Si TFT is used as n-type MOSFET while p-type MOSFET are used as complementary devices.

4. Detailed Designed Procedure

The design procedure of proposed Op-amp is described in Figure 4 and required basic fundamental data is given in Table 1. The design procedure carried out for the Op-amp using a-Si TFT as n-MOS transistor and p-MOS transistor. Also, the design procedure and simulation for CMOS Op-Amp have been carried out. Simulation results are used here to compare and analyze their performance along with the existing work.

- (1) Determine I_{D5} from the SR specification. Let $C_c = 1pF$,
 $SR = I_{SD5} / C_c$ $I_{SD5} = (SR)(C_c)$

$$\text{or } I_{SD5} = \frac{K_N V_{eff}^2}{2} = \frac{(1.35 \times 10^{-6})(1.8^2)}{2}$$

$$= (2.187 \times 10^{-6}) = 2.2\mu A$$

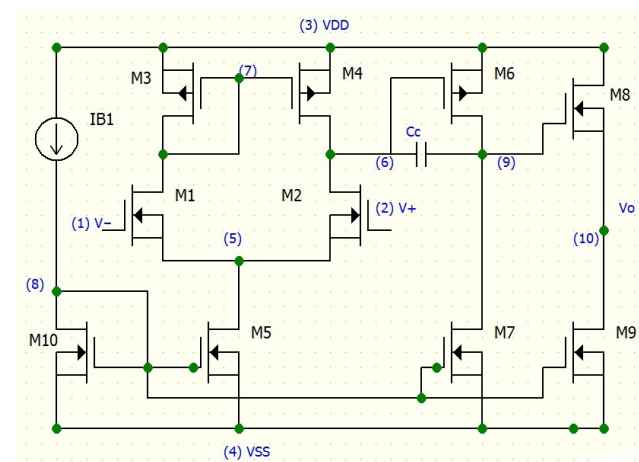


Figure 3. Two stage Op-Amp with n-channel input stage.

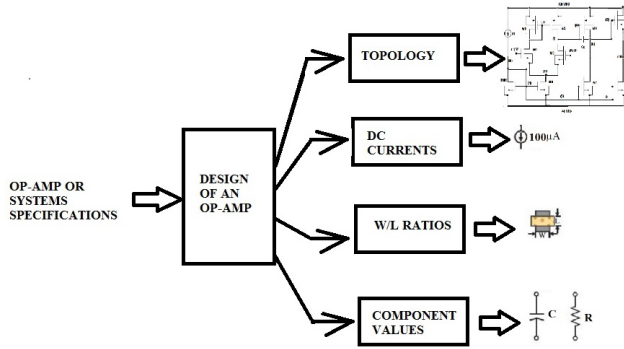


Figure 4. Design procedure of an Op-Amp.

$$SR = I_{SD5} / C_C = 2.0 \times 10^{-6} / 1 \times 10^{-6} = 2.2V / \mu S$$

$$V_{SD5(SAT)} = V_{SG5} - |V_{TPO}| = V_{DD} - V_{bias} - |V_{TPO}| = 3 - 1.7 - |1.0| = 0.3$$

$$\left[\frac{W}{L} \right]_5 = \frac{2I_{SD5}}{K_N V_{SD5(SAT)}^2} = \frac{2(2.2E-6)}{(1.35E-6)(0.3)^2} = 36.2139 = 37.0$$

$$I_{SD1} = I_{SD2} = \frac{I_{SD5}}{2} = \frac{2.2}{2} = 1.1 \mu A$$

(2) Determine $(W/L)_1$ from the W_{GB} and positive CMR specification. From W_{GB} specification,

$$W_{GB} = \frac{g_{m1}}{C_c} = \frac{1}{C_c} \sqrt{2K_N (W/L)_1 I_{SD1}}$$

$$g_{m1} = C_c W_{GB} = (1E-12)(2\pi \times 150E+03) = 0.9425 \mu mho \approx 1.0 \mu mho$$

Table 1. Design Parameter

DESIGN AND SPICE PARAMETERS			
VDD	+3V	VSS	-3V
Ao	≥1000	GB	2π(20KHz)
SR	2.2V/μS	PM	>85°
Ro	≤1.5K	Λ	0.04
Veff	1.8V	-2.65 ≤ CMR ≤ 0.65	
Cox	135 E-6 FM-2	Kn = μn X Cox	1.35uA/V2
μn	100 E-4 M²/VS	Kp	48.74 uA/V2

$$\left(\frac{W}{L} \right)_1 = \frac{(g_{m1})^2}{2K_N I_{SD1}} = \frac{[1.0E-6]^2}{2(1.35E-6)(1.1E-6)} = 0.3367$$

From the positive CMR specification,

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - V_{SG1}$$

$$V_{SG1} = V_{DD} - V_{SD5(SAT)} - V_{G1(max)}$$

From the gate bias V_{bias} , V_{SD5} can be determined.

$$V_{SG1} = V_{DD} - V_{SD5(SAT)} - V_{G1(max)} = 3 - 0.3 - 1.4 = 1.3$$

$$V_{SD1(SAT)} = V_{SG1} - |V_{TP0}| = 1.3 - |-1| = 0.3$$

$$\left(\frac{W}{L} \right)_1 = \frac{2I_{SD1}}{K_N V_{SD1(SAT)}^2} = \frac{2[1.1E-6]}{(1.35E-6)(0.3)^2} = 18.11$$

To satisfy both specifications select the higher (W/L) ratio. For matching and symmetry, we also choose $(W/L)_2 = (W/L)_1 = 18.11$.

(3) Determine $(W/L)_3 = (W/L)_4$ ratio from negative CMR

$$\left(\frac{W}{L} \right)_3 = \frac{2I_{SD3}}{K_P (V_{G1(min)} - V_{SS})^2} = \frac{2[1.1E-6]}{(48.74E-6)(-2.80 - (-3))^2} = 1.1284 = 1.1 = \left(\frac{W}{L} \right)_4$$

(4) Determine $(W/L)_6$ from the $PM > 89^\circ$ specification.

$$PM = 90 - \tan^{-1}(W_{GB} / z) - \tan^{-1}(W_{GB} / p_2)$$

$$W_{GB} = \frac{g_{m2}}{C_c}; z = \frac{g_{m6}}{C_c}; p_2 = \frac{g_{m6}}{C_1 + C_2}; z < p_2;$$

Since $C_c > C_1 + C_2$

An estimate of PM is obtained by assuming $z = p_2$. That is

$$PM < 90 - 2 \tan^{-1} \left(\frac{g_{m2}}{C_c} / \frac{g_{m6}}{C_c} \right)$$

$$= 90 - 2 \tan^{-1} \left(\frac{g_{m2}}{g_{m6}} \right)$$

$$\tan^{-1} \left(\frac{g_{m2}}{g_{m6}} \right) < \frac{90 - PM}{2} \quad \frac{g_{m2}}{g_{m6}} < \tan \left(\frac{90 - PM}{2} \right)$$

$$g_{m6} > g_{m2} / \tan \left(\frac{90 - PM}{2} \right)$$

$$g_{m6} > \frac{1.0E-6}{\tan\left(\frac{90-89}{2}\right)} = 114.6E-6 \approx 110E-6$$

From step 4, $V_{SD6(SAT)} = V_{SD3(SAT)} = 0.08V$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{K_P V_{SD6(SAT)}} = \frac{[110E-6]}{(48.74E-6)(0.08)} \\ = 14.11 \approx 14.5$$

The current through M6 is given by

$$I_{SD6} = \frac{g_{m6}^2}{2K_P (W/L)_6} = \frac{[110E-6]^2}{2(48.74E-6)(14.5)} \\ = 8.56\mu A \approx 8.6\mu A$$

For balance condition the current through M_6 must be properly ratioed with the current through M_3 ,

$$I_{SD6} = \frac{(W/L)_6}{(W/L)_3} I_{SD3} = \frac{14.5}{1.1} (1.1\mu A) \\ = 14.5\mu A \approx 14.0\mu A$$

To satisfy the condition, we also choose higher value of the current through M_6

(5) Determine $(W/L)_7$ from the condition and that is

$$I_{SD7} = I_{SD6}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_{SD7}}{I_{SD5}} \left(\frac{W}{L}\right)_5 = \frac{14.0\mu A}{2.2\mu A} (37.0) \\ = 235.45 \approx 236$$

(6) DC gain A_{V0} is computed and compared with the specification:

$$A_{V0} = g_{m2} g_{m6} R_1 R_2 = \frac{g_{m2} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})} \\ = \frac{g_{m2} g_{m6}}{(\lambda_2 + \lambda_4) I_{SD2} (\lambda_5 + \lambda_6) I_{SD6}} \\ = \frac{(1.0E-6)(110E-6)}{(0.04 + 0.04)(1.1E-6)(0.04 + 0.04)(14.0E-6)} \\ = 7,102 \geq 10,000$$

(7) From the output resistance specification $R_o \leq 1.5k$, $(W/L)_8$ can be determined. The output resistance is given by:

$$R_o = \frac{1}{g_{m8}} = \sqrt{\frac{1}{2\beta_8 I_{SD8}}} = \sqrt{\frac{1}{2K_N (W/L)_8 I_{SD8}}}$$

Solving for $(W/L)_8$, assuming $I_{SD8} = 75\mu A$ and HSpice parameter $K_N = 1.35\mu A/V^2$

$$(W/L)_8 = \frac{1}{2K_N R_o^2 I_{SD8}} \\ = \frac{1}{2(1.35E-6)(1342)^2 (75E-6)} \\ = 2742.01 \approx 2742.0$$

(8) Determine the (W/L) of the current mirrors. First set up the current source M_{10} to $100\mu A$ using the biasing current source IB. The V_{GSS} is set up to guarantee it and operates at saturation by adding $-0.5V$ beyond its threshold voltage of $V_{tp} = -1V$. That is $V_{SG10} = 2.5V$. $(W/L)_{10}$ can now be determined as follows:

$$(W/L)_{10} = \frac{2I_{SD10}}{K_N (V_{GS10} - |V_{tp}|)^2} \\ = \frac{2(100E-6)}{(1.35E-6)(2.45 - |-1.5|)^2} \\ = 164.16$$

The rest of current sources are determined by proportionality as follows:

$$I_{SD10} = 100\mu A \Rightarrow (W/L)_9 \\ = (W/L)_{10} (I_{SD9} / I_{SD10}) \\ = (164.16)(100\mu A / 100\mu A) = 164.16$$

Here this procedure completes the design. The results are summarized in the Table-2a and 2b:

Adjusted to satisfy the balance condition to minimize the input offset voltage, V_{os} :

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$

The design has been simulated in HSPICE Circuit Simulator using Table-2a and Table-2b. The simulation result of DC offset voltage of a-Si TFT Op-Amp is shown in Figure 5a while the result of CMOS Op-Amp is shown in Figure 5b. The arrow shown in Figure 5a, shows that the output voltage $V_o = V_{10}$ is $58.1174mV$ at quiescent operating point. This offset is determined by finding the value of VID that makes the output voltage $V_o = V(10) = 0$. From

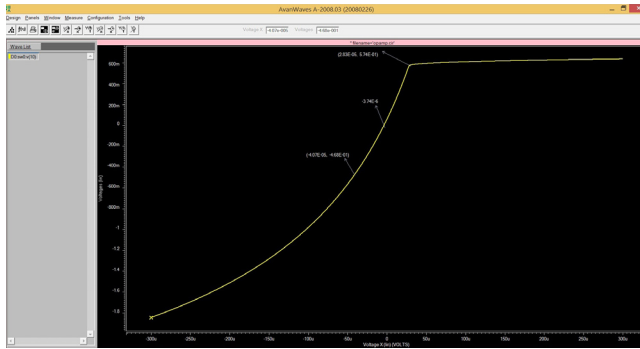


Figure 5. (a) DC offset voltage: a-Si TFT Op-Amp.

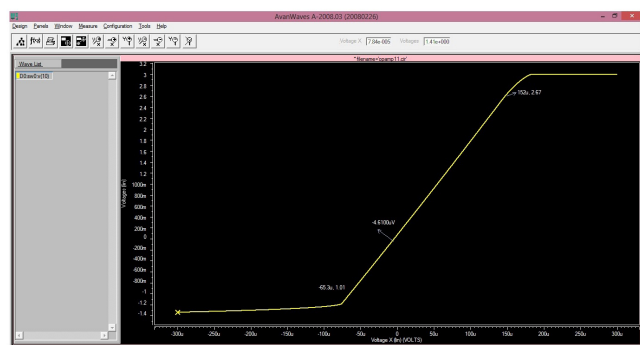


Figure 5. (b) DC offset voltage: CMOS Op-Amp.

the above graph, this is obtained as $-3.74\mu\text{V}$. The resulting output voltage after modifying the VID in the net list of simulation is $-688.7476\text{E-}6\text{V}$.

The differential gain can be obtained from the DC transfer characteristic by locating two points centered about the bias point of $\text{VID} = V_{\text{os}} = -3.74\mu\text{V}$. For accuracy, the two points must be far apart. From the graph:

$$A_{\text{VD}} = \frac{(5.74 \times 10^{-1}) - (-4.68 \times 10^{-1})}{(2.83 \times 10^{-5}) - (-4.07 \times 10^{-5})} = 1.51015 \times 10^4$$

This value is very closer to the value obtained in simulation using TF analysis, which is 15.1003K .

The common-mode input range is determined when the output cease to follow the input linearly. At the low end, it determines $V_{\text{G1(MIN)}} = -0.0105$, and at the high end, it determines $V_{\text{G1(MAX)}} = 0.501\text{V}$. These are very close to the corresponding design specifications of $V_{\text{G1(MIN)}} = -0.0105$ and $V_{\text{G1(MAX)}} = 0.0501\text{V}$. The common-mode gain is obtained by locating two points as far apart in the linear range about the operating point. This is shown in Figure 6a,

while the graph of CMOS Op-Amp is shown in Figure 6b and computed as follows:

$$A_{\text{CM}} = \frac{0.585 - (-0.101)}{0.0501 - (-0.0105)} = 11.3388$$

This value is much near to the value obtained in simulation using the TF analysis of 11.5409 . The common mode rejection ratio CMRR is calculated as follows:

$$\text{CMRR} = \frac{A_{\text{VD}}}{A_{\text{CM}}} = \frac{15.1003 \times 10^3}{11.5409} = 1.3317\text{K}$$

The Op-Amp frequency response of a-Si TFT Op-Amp obtained is shown in the Figure 7a (The graph of CMOS Op-Amp is shown in Figure 7b) and the HSpice simulation results are $A_{\text{V0}} = 1.2496\text{E}+3$, Phase Margin $= 80^\circ$ and $f(\text{GB}) = 1.35\text{MHz}$

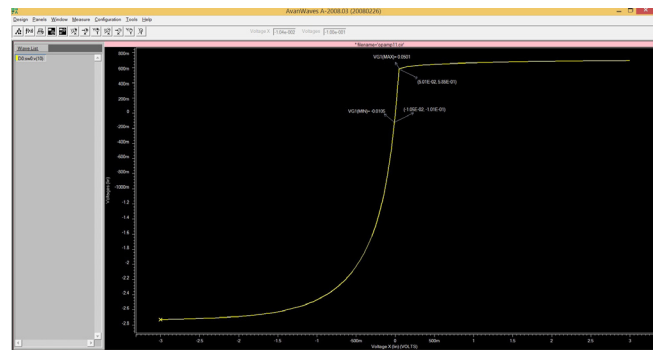


Figure 6. (a) Common mode voltage range determination: a-Si TFT Op-Amp.

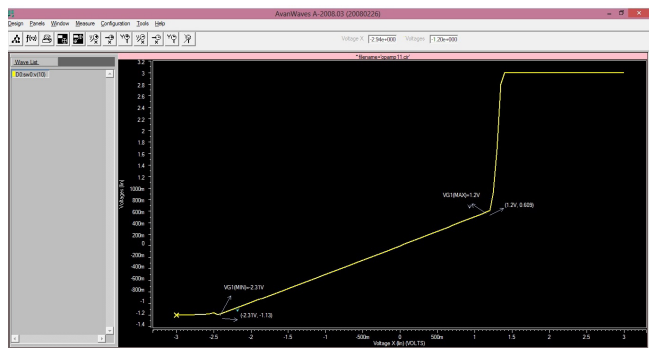


Figure 6. (b) Common mode voltage range determination: CMOS Op-Amp.

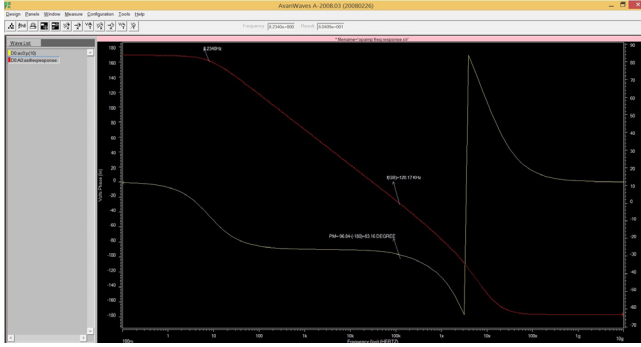


Figure 7. (a) Frequency response: phase and magnitude plot of a-Si TFT Op-Amp.

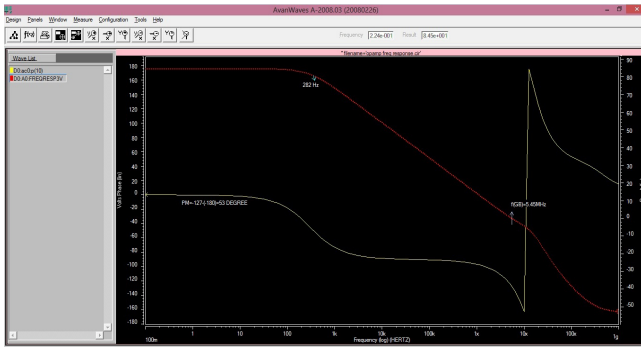


Figure 7. (b) Frequency response: phase and magnitude plot of CMOS Op-Amp.

The theoretical bandwidth and gain bandwidth are calculated as follows:

$$g_{m1} = 9.43 \times 10^{-6} \text{ umho}$$

$$g_{m2} = 16 \times 10^{-6} \text{ umho}$$

$$R_1 = \frac{1}{(\lambda_1 + \lambda_2)I_2} = \frac{1}{(0.02 + 0.02)(3.5 \times 10^{-6})} = 7.143 \times 10^6 = 7.143 \text{ M}$$

$$R_2 = \frac{1}{(\lambda_6 + \lambda_7)I_6} = \frac{1}{(0.02 + 0.02)(35 \times 10^{-6})} = 0.714 \times 10^6 = 0.714 \text{ M}$$

$$p_1 = \frac{-1}{g_{m1}R_1R_2C_C} = \frac{1}{(9.43 \times 10^{-6})(7.143 \times 10^6)(0.714 \times 10^6)(1 \times 10^{-12})} = 0.02079 \times 10^6 = 2079$$

$$f_1 = \frac{p_1}{2\pi} = \frac{2079}{2\pi} = 331.1 \text{ Hz}$$

$$f_{GB} = A_{VO}f_1 = (1.2496 \times 10^3)(835) = 1.0434 \text{ MHz}$$

$$z = \frac{g_{m6}}{C_C} = \frac{16 \times 10^{-6}}{1 \times 10^{-12}} = 16 \times 10^6$$

$$f_z = \frac{z}{2\pi} = \frac{16 \times 10^6}{2\pi} = 2.55 \text{ M}$$

Simulation results of a-Si TFT Op-Amp at $f_1 = 8.234 \text{ Hz}$, $f_{GB} = 120.17 \text{ kHz}$, f_z and f_2 are difficult to obtain accurately from bode plot.

The positive slew rate is the slope of the rising edge of the output in Figure 8a and Figure 8b. This is computed from the two points on the rising edge. That is,

$$SR = \frac{0.8019 - (-2.7078)}{11.258 - 10.366} = 3.9346 \text{ V} / \mu\text{s}$$

Similarly, the new slew rate is computed as follows:

$$SR = \frac{-1.5952 - 0.6385}{49.7690 - 43.7790} = -0.3729 \text{ V} / \mu\text{s}$$

5. Results and Discussion

Two Operational Amplifiers of a-Si TFT and CMOS transistors are well described and their specification used for are shown in Table 1, Table 2A and Table 2B. Using HSpice Circuit Simulator, the graph has been recorded and summarized in the Table -3 and 4 for comparing both the Operational Amplifiers. Figure 5a and 5b shows the transient responses to calculate DC offset voltage and

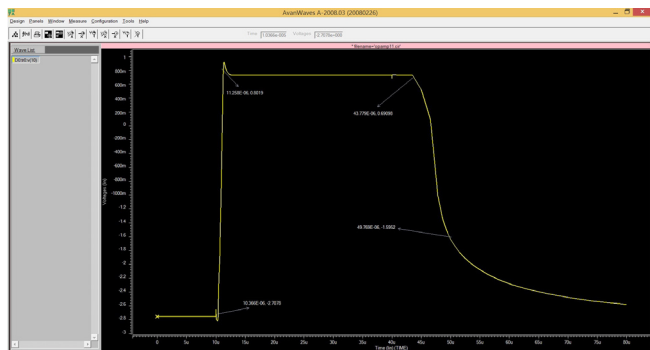


Figure 8. (a) Slew rate measurement: a-Si TFT Op-Amp.

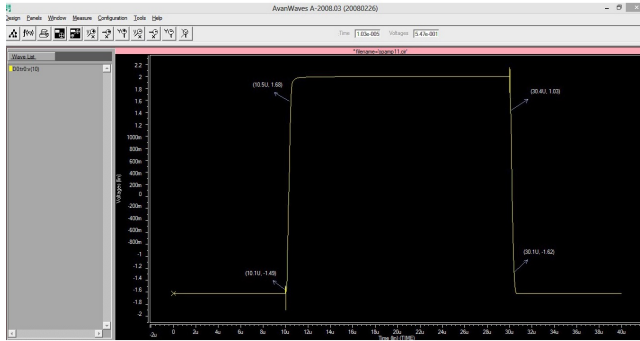


Figure 8. (b) Slew rate measurement: CMOS Op-Amp.

Table 2. (a) Design Specification of- Si TFT Op-Amp ($L=6.6\mu\text{m}$ are used)

PAR	Values Obtained After Calculation			Values of W and L after adjusting to Nearest Multiple of $\lambda=0.6$, and Obtaining Balancing Conditions		
	I (Ua)	W/L	W (μm)	I (Ua)	W/L	W (μm)
M1	1.1	18.11	101.4	0.9619	18.85	105.9
M2	1.1	18.11	101.4	0.9619	18.85	105.9
M3	1.1	1.11	6.2	0.9619	1.11	6.2
M4	1.1	1.11	6.2	0.9619	1.11	6.2
M5	2.2	37.0	207.2	1.9240	37.5	210.0
M6	14	14.5	81.2	12.03	14.5	81.2
M7	14	236	1321.6	12.03	21.2	118.8
M8	75	2709.6	15173.8	75.33	2742.7	15359.1
M9	75	164.16	991.3	75.33	166.6	933.0
M10	100	164.16	991.3	100	166.6	933.0

differential voltage gain. Figure 6a and 6b shows the plot for common mode voltage range and determined the common mode voltage gain and computed the CMRR value. Figure 7a and 7b shows the frequency response curve as phase plot and magnitude plot, there by calculated the Unity Gain Bandwidth and Phase Margin. Figure 8a and 8b shows the transient response to the pulse input voltage for computing the positive slew rates.

6. Conclusion

Differential amplifiers with accurately balanced outputs can be easily realized if the differential-mode circuitry and the common-mode circuitry are treated equally in the design process. A convenient way of accomplishing

Table 2. (b) Design Specification of Cmos Op-Amp ($L=6.6\mu\text{m}$ and $L_{\text{eff}}=5.6\mu\text{m}$ are used)

PAR	Values Obtained After Calculation			Values of W and L after adjusting to Nearest Multiple of $\lambda=0.6$, and Obtaining Balancing Conditions		
	I (Ua)	W/L	W (μm)	I (Ua)	W/L	W (μm)
M1	5	6.57	36.9	6.6	5.6	5
M2	5	6.57	36.9	6.6	5.6	5
M3	5	1	3.9	6.6	5.6	5
M4	5	1	3.9	6.6	5.6	5
M5	10	5.333	29.87	6.6	5.6	10
M6	30	6	33.6	6.6	5.6	30
M7	30	16	89.6	6.6	5.6	30
M8	100	156	873.6	6.6	5.6	100
M9	100	53.33	296.86	6.6	5.6	100
M10	100	53.33	296.86	6.6	5.6	100

Table 3. Transistors Aspect Ratio and Their Function Op-Amp

Transistors	Aspect Ratio ($L = 6.6\mu\text{m}$)		Function	Region of Operation
	Poly-Si TFT	CMOS		
M1 & M2	105.9 μm & 105.9 μm	36.6 μm & 36.6 μm	Input drivers	Saturation
M3 & M4	6.2 μm & 6.2 μm	5.4 μm & 5.4 μm	Current mirror Active load to differential gain stage	Saturation
M5	210 μm	31.3 μm	Bias current Source	Linear
M6	81.2 μm	32.4 μm	Active load of second stage	Saturation
M7	118.8 μm	90 μm	Second stage driver	Saturation
M8 & M9	15359.1 μm & 933.0 μm	873.6 μm & 300 μm	Current Buffer	Saturation
M10	933.0 μm	300 μm	Current mirror active load	Saturation

Table 4. Performance of Op-Amp after Simulation

Parameters	Simulation Results	
	A-Si TFT	CMOS
Gain	15.1003k	16.7618 K
UGB	120.17KHz	5.45MHz
CMRR	1.3317K	34.182K
Slew Rate	3.9346V/ μ S	7.925V/ μ S
Dc Offset Voltage	-688.7476 μ V	197.6208 μ V
Power Dissipation	1.1357m.Watts	1.4690 m. Watts
Output Resistance	10.1345K	1.3919 K
Phase Margin	83.16°	54°
Open loop Gain Margin	83.6dB	84.5dB

this is to use a topology that combines the two parts as close as possible to the front end of the amplifier. In this way most of the design issues such as gain, compensation, etc. are addressed at the same time for both the differential and common-mode signal paths. The design strategy discussed in this paper has been verified with both a-Si TFT and CMOS Op-Amp. Power dissipation is relatively high on both the OP-Amps, while using a large transistor at M_8 . Simulation results indicate that a-Si TFT is performing well and shows good agreement with existing work. Unity Gain Bandwidth of a-Si TFT Op-Amp is very less, 120KHz compared to CMOS Op-Amp. While performance of CMOS Op-Amp is better in slew rate, UGB and CMRR while compared to a-Si TFT Op-Amp.

Output resistance and Phase Margin of a-Si TFT Op-Amp is better compared to CMOS Op-Amp which indicates that the stability of a-Si TFT is better and shows good agreement with the existing work²³.

7. References

- Matsuo T, Muramatsu T. 21.1:Invited paper: CG silicon technology and development of system on panel. SID Symposium Digest of Technical Papers; 2004 Jul 5. p. 856–9. doi: 10.1889/1.1821405.
- Brotherton S, McCulloch D, Clegg J, Gowers J. Excimer-laser-annealed poly-Si thin-film transistors. *Electron Devices, IEEE Transactions*; 1993; 40(2):407–13. doi:10.1109/16.182521.
- Sposili RS, Im JS. Sequential lateral solidification of thin silicon films on SiO₂. *Applied Physics Letters*. 1996; 69(19):2864–6. Available from: <http://dx.doi.org/10.1063/1.117344>.
- Voutsas AT. Assessment of the performance of laser-based lateral-crystallization technology via analysis and modeling of poly-silicon thin-film-transistor mobility. *Electron Devices, IEEE Transactions*. 2003 Jun; 50(6):1494–500. doi:10.1109/TED.2003.813347.
- Tarn YC, Ku PC, Hsieh HH, Lu LH. An amorphous silicon operational amplifier and its application to 4 bit digital to analog converter. *IEEE Journal Solid State Circuits*. 2010 May; 45(5):1028–35. doi:10.1109/JSSC.2010.2043886.
- Allee DR, Venugopal SM, Krishna R, Kafthanoglu K, Quevedo M, Gowrishankar S, Avendano-Bolivar AE, Alshareef HN, Gnade B. Flexible CMOS and electrophoretic display. *Society for Information Displays, International Symposium Digest of Technical papers*; 2009 Jun; San Antonio, Texas. p. 45–54.
- Johns DA, Martin K. *Analog integrated circuit design*; 1997; New York, Wiley.
- Palmisano G, Palumbo Pennisi S. Design procedure for two-stage CMOS transconductance operational amplifiers: a tutorial. *Analog Integrated Circuits and Signal Processing*. 2001 May; 27(3):179–89. doi:10.1023/A:1011229119071.
- Mahattanakul J, Chutichatuporn J. Design Procedure for Two-Stage CMOS OPAMP with Flexible Noise-Power Balancing Scheme. *IEEE Transaction on Circuits and Systems-I: Regular Paper*; 2005 Aug; 52(8):1508–14. doi:10.1109/TCSI.2005.851395.
- AmanaYA. Review paper on design and synthesis of two-stage CMOS Op-Amp. *International Journal of Advances in Engineering and Technology*. 2012 Jan; 1(6):677–88. ISSN: 2231-1963.
- Ramirez-Angulo J. Low-voltage, low-power rail-to-rail two stage op-amp with dynamic biasing and no Miller compensation. *Proceeding of the 50th Midwest Symposium on Circuits and Systems, MWSCAS*; 2007 Aug 5-8; Quebec, Canada. p. 25–8.
- Rosario M, Gaetano P, Salvatore P. Design guidelines for reversed nested miller compensation in three-stage amplifiers. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*. 2003 May; 50(5):227–33. doi:10.1109/TCSII.2003.811437.
- Singh R, Anu G. Design on fully differential Op-amp for high stability. *Proceedings of the International Conference on Electric and Electronic*; 2011; Coimbatore, India. p. 1–5.
- Vaibhav K, Degang C. Design procedure and performance potential for operational amplifier using indirect compensation. *Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems*; 2009 Aug 2-5; Cancun, Mexico; p. 13–6.
- Pugliese A, Amoroso FA, Cappuccino G, Cocorullo G. Settling-time-oriented design procedure for two-stage

- amplifiers with current-buffer Miller compensation. Proceeding of the 4th European Conference on Circuits and Systems for Communications; 2008 Jul 10–11; Bucharest, Romania; p. 114–17. doi:10.1109/ECCSC.2008.4611658.
16. Gupta A. A two stage and three stages CMOS OPAMP with fast settling, high DC gain and low power designed in 180nm technology. Proceedings of the International Conference on Computer Information Systems and Industrial Management Applications (CISIM); 2010 Oct 8–10; Venice, Italy; p. 448–53. doi:10.1109/CISIM.2010.5643497.
17. Jin F, Fu X, Niu P, Yang G, Gao T. The research of operational trans-conductance amplifier. Proceeding of the International Conference on IEEE Control, Automation and Systems Engineering (CASE); 2011 Jul 30–31; Singapore. p. 1–4.
18. Prabhakaran G, Kannan V. Analysis and modelling of hybrid operational amplifiers using amorphous silicon thin film transistor. CiiT International Journal of Programmable Devices Circuits and Systems. 2011 Sep; 3(12). doi: PDCS092011007.
19. Prabhakaran G, Kannan V. Design and analysis of hybrid operational amplifiers using poly-si thin film transistor for low voltage applications. Proceedings of International Conference on Global Innovations in Technology and Sciences. Published in International Journal of Scientific and Engineering Research (IJSER). 2013 Apr 4–6; 4(8). ISSN 2229-5518.
20. Prabhakaran G, Kannan V. Low voltage application of hybrid Op-Amp using thin film transistor in summing amplifier. Ciencia e Tecnica Vitivinicola Journal. 2014; 29(7). ISSN: 0254-0223.
21. Prabhakaran G, Kannan V. Design configuration of circuit and comparison of hybrid TFT Op-Amp with its CMOS Counterpart. Paper presented at 2nd National Conference on Advancements and Future Trends in VLSI Design (NCVD'14) in Kalasalingam University; 2014 Sep 26. p.1–9. Published in International Journal of Digital Communication and Networks (IJDCN); 2014 Sep; 1(3). ISSN: 2345-9850. Available from: <http://ijdcn.co.in/issue-category/volume-3-september-2014>.
22. Prabhakaran G, Kannan V. Design and Analysis Of Thinfilm Transistor Based Operational Amplifier. Sylwan Journal. 2015 Jan; 159(1). ISSN: 0039-7660.
23. Reay RJ, Kovacs GTA. An unconditionally stable two-stage CMOS amplifier. IEEE Journal Solid-State Circuits. 1995 May; 30(5):591–4. ISSN 0018-9200 CODEN: IJSCBC.