Indian Journal of Science and Technology, Vol 8(14), DOI: 10.17485/ijst/2015/v8i14/62716, July 2015
ISSN (Print) : 0974-6846
ISSN (Online) : 0974-5645

Design and Analysis of Low Power Memory Built in Self Test Architecture for SoC based Design

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Abstract

This paper targets on the low power design of Memory Built In Self Test (MBIST) architecture for System on Chip (SoC) based design. Proposed address generator is developed with the blend of gray code counter and modulo counter. Bit reversing technique is adopted in this paper to generate the last pattern of gray code counter. In this work a refined architecture of MBIST is also constructed by embedding a low power address generator in it. Efficient employment of the proposed address generator in MBIST has cut-down the power consumption of BIST architecture compared to the traditional BIST. Reduction of about 6% of switching activity has been observed with novel MBIST architecture.

Keywords: Gray Code, Low-Power, MBIST, Modulo Counter, MUT

1. Introduction

It is evident that the power consumption in test application mode is resulted more compared to the normal operating mode. The main reason is that the correlation in test patterns are lesser in testing mode compared that in normal mode. If the power consumed during the testing mode exceeds the power constraint of the chip, then the chip may become structurally degraded and may be damaged[1]. The overall power consumption in a system on chip is contributed by both static power when the system is in standby mode and dynamic power when the system is in working mode. Dynamic power is resulted mainly due to the switching activity in the circuit. It can be mathematically represented as follows.

$$P_{avg} = \alpha T \; C_{load} V^2_{dd} f_{clk}$$

Where
αT Switching activity factor of the gate
C_{load} Total load capacitance
V_{dd} Supply voltage
f_{clk} Operating frequency

From the above equation, it is evident that the average power consumption is in direct relation with switching activity in the system. And for a low power designs this switching activity has to be cut down drastically to minimize the dynamic power consumption. This power is twice when the system is under test as the consecutive test patterns are applied to the memory cores for diagnosing faults in memory.

The production of complex designs has been increasing in recent years. These complex designs have to be verified and tested to assure their functionality when it comes to the user end. It results in the hike of development cost which is in direct relation to the complexity of the system. Plenty of external testing techniques are available in market but with less reliability. The main drawback with external testing is that the failures in the system can only be identified after its effect has been witnessed by the

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developer or user. So, it is important to identify the failure in the system before facing their consequences.

Built In Self Test (BIST) techniques are found to be better alternative compared to external testing as they provide on chip test pattern generation and response analysis. This efficient employment of BIST may reduce external testing expenses and also test time. The logic blocks which are embedded in VLSI chips usually have low observability and controllability which results in less fault coverage. BIST techniques are optimal for testing such embedded cores.

But disadvantage of employing BIST in a system is that it draws excessive power during application of test patterns to the input of Circuit Under Test (CUT)[2]. The main reason behind this is that during the testing mode, the switching activity is higher comparatively to the normal mode[3].

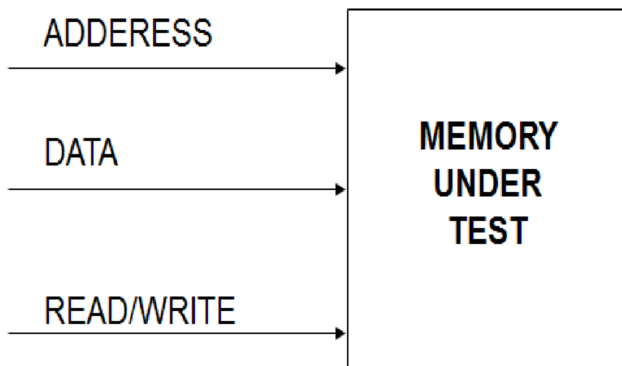


Figure 1. General testing scheme for memory under test.

As shown in the Figure 1 memory under test has to be accessed consecutively to write the test data and read the test data. This requires every address of the memory to be generated simultaneously which causes higher switching between the addresses. This switching activity consumes major part of the power supply which is not an encouraging factor for low power devices. Address generator plays a key role in the cause for switching activity.

So, there is a need to employ an address generator in such a way that it has minimal switching in the consecutive output patterns. Generally Linear Feedback Shift Register (LFSR) is employed as an address generator as it occupies lesser area overhead. But it resulted in higher dynamic power consumption due its rapidity of switching in the output.

Gray code counters provide the least output switching patterns that are best suitable for low power on chip BIST employment. Binary counter and a series of eXclusive-OR gates forms a typical gray code generator. Gray sequence generators can be implemented by modifying counters that may exist in the circuit[4].

2. Related Works

Hierarchy of address generators start with a normal binary up-down counter that produce sequence of addresses. When area and power are concerned, binary up-down counters occupy more area and also consumes more power. To overcome the area problem, LFSR's were introduced. It succeeded in scaling down the area occupied by address generators. But it failed to answer the power consumption caused by switching activity.

Several algorithms were later introduced to cut down the switching in LFSR. In Bit-swapping LFSR[5] comprise traditional LFSR and 2:1 multiplexers. The selector line of the MUX is chosen if the Nth bit position value is '0' and accordingly, the bits linked to the MUX are swapped otherwise i.e. if the Nth bit position value is '1' nothing occurs, the series thus produced have a superior switching activity than the traditional LFSR. To overcome power consumption problem, diverse kinds of address generators are found employed for MBIST. In a programmable MBIST, two counters and multiplexer combination are employed as an address generator[6].

The work proposed in[13] concentrates on improving the hardware in terms of area and number of logical gates in the 2-D LFSR used for testing an SoC with multiple IP cores so that vectors in various patterns can be generated using a single reconfigurable two Dimensional LFSR.

A new hamming model has proposed[14] to overcome the scan based attack and not to give any correlation relationship in hamming distance by providing the similar intermediate values for all test vector patterns which are obtained through an optimal way of inserting Optimal Scan Flip Flop (OSFF) randomly to the scan path chain.

A new reseeding technique with a considerable scan power reduction was proposed earlier[7]. The reseeding is applied on general LFSR and modified LFSR in two ways. These generated patterns are sent to a XOR network which will generate an output. A new LFSR reseeding technique for efficient reduction of test pattern was proposed by S. Saravanan and Har Narayan Upadhyay[8]. A new encoding technique to reduce the size of the test data was proposed in this study. Size of the test data was

reduced by clock in LFSR which is in the state of inactive for several clock cycles after the seed is given to the input. When the clock enters inactive state, a right shift rotate operation is carried on the seed to get the remaining possible values. After acquiring all the possible data for that particular seed, a new seed is inserted by making the clock to be active. Thus reduction in test data volume is achieved by storing the data only when the clock is in active state. All the remaining test vectors were derived with in the reduced clock.

In certain other cases, Binary up-down counter and Gray code Counters are employed as address generators[9]. With a concern to still decrease the switching activity, in our work, we have developed and executed a new address generator which uses bit reversal technique along with a modulo counter and grey code convertor.

3. Proposed Method

Linear Feedback Shift Registers (LFSR) or counters generally employed as address generators for memory locations, need to be investigated for flaws. The traditional LFSR is incapable of producing the entire zero patterns because when all the flip-flop output becomes zero then the XOR output is also zero hence the feed backs to the 1st flip-flop input are also zero, hence the LFSR becomes stuck at zero stage. To overcome this problem, a Complete Memory Address Generator (CMAG)[10] was proposed in previous works. But power consumption is considerably high when traditional architectures are employed as address generators. To overcome the power consumption problem, a novel architecture is introduced.

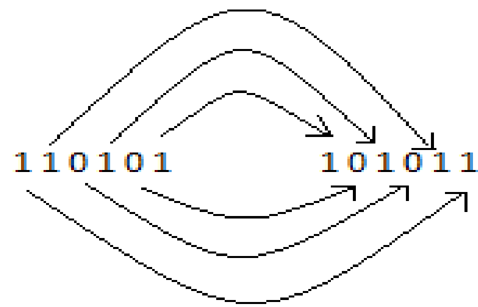


Figure 2. Reversible Pattern.

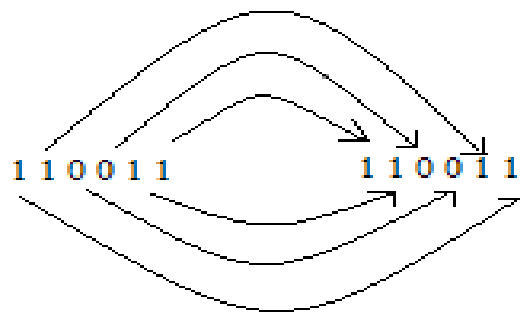


Figure 3. Irreversible Pattern.

The architecture of address generator proposed in this paper is a blend of modulo counter and gray code convertor with a blend of bit reversal block. This paper focuses mainly on utilizing the reversible bit patterns. That is when we look at the patterns, we come across certain pat-

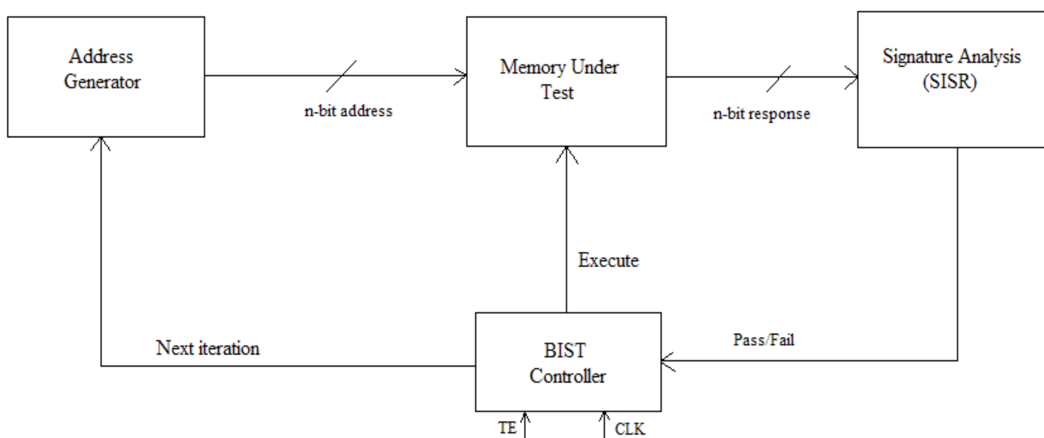


Figure 4. Proposed MBIST Architecture.

terns which can be reversible. For example, 0000000001 is a pattern which is reversible. When certain pattern is reversed, the other address or pattern, 1000000000 can be obtained. An example for such a reversible pattern is shown in the Figure 2.

There exists certain other patterns which cannot be reversed. For example, 1000000001 or 1001001001 are some patterns which results in the same pattern even if we reverse them. An example for such an irreversible pattern is shown in the Figure 3.

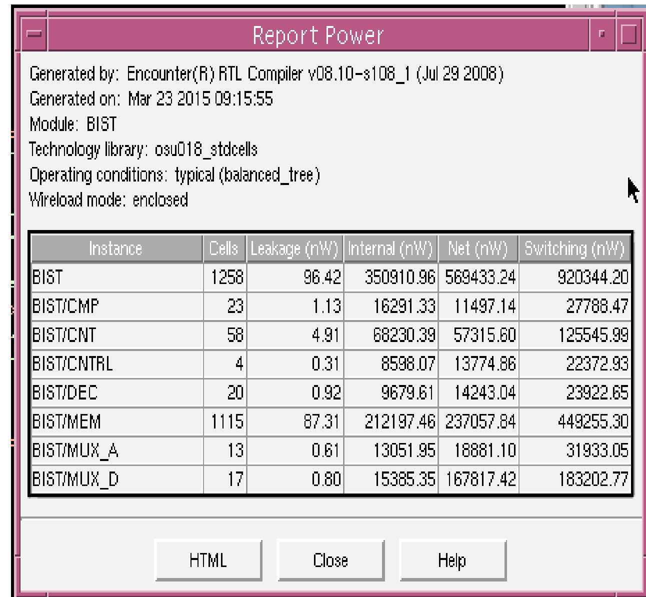
Employing this novel low transition address generator in a MBIST (Memory Built-In Self-Test) architecture as shown in the Figure 4 resulted in reduced power consumption compared to the conventional MBIST using LFSR as an address generator.

4. Results and Comparison

The test outcomes of the proposed architecture resulted in reduced power when analyzed with supporting EDA tools. Here, we have taken pains to implement the proposed design of address generator in Xilinx ISE design tool and analyzed the dynamic power and also the total power consumption using Xpower analyzer. And further the designed address generator have embedded in a BIST architecture and compared the power consumption with conventional BIST having LFSR as an address generator. This has done in cadence RTL Compiler.

The comparison of both dynamic power and total power consumption of conventional MBIST architecture which uses LFSR as address generator with proposed architecture has been tabulated in the Table 1.

Thus the designed address generator is embedded in a BIST architecture and is synthesized using cadence RTL compiler which resulted in low power consumption compared to the conventional BIST architecture which uses LFSR as an address generator. The Figure 5 and Figure 6 shows the results from RTL compiler.



Report Power

Generated by: Encounter(R) RTL Compiler v08.10-s108_1 (Jul 29 2008)
Generated on: Mar 23 2015 09:15:55
Module: BIST
Technology library: osu018_stdcells
Operating conditions: typical (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
BIST	1258	96.42	350910.96	569433.24	920344.20
BIST/CMP	23	1.13	16291.33	11497.14	27788.47
BIST/CNT	58	4.91	68230.39	57315.60	125545.99
BIST/CNTRL	4	0.31	8598.07	13774.86	22372.93
BIST/DEC	20	0.92	9679.61	14243.04	23922.65
BIST/MEM	1115	87.31	212197.46	237057.84	449255.30
BIST/MUX_A	13	0.61	13051.95	18881.10	31933.05
BIST/MUX_D	17	0.80	15385.35	167817.42	183202.77

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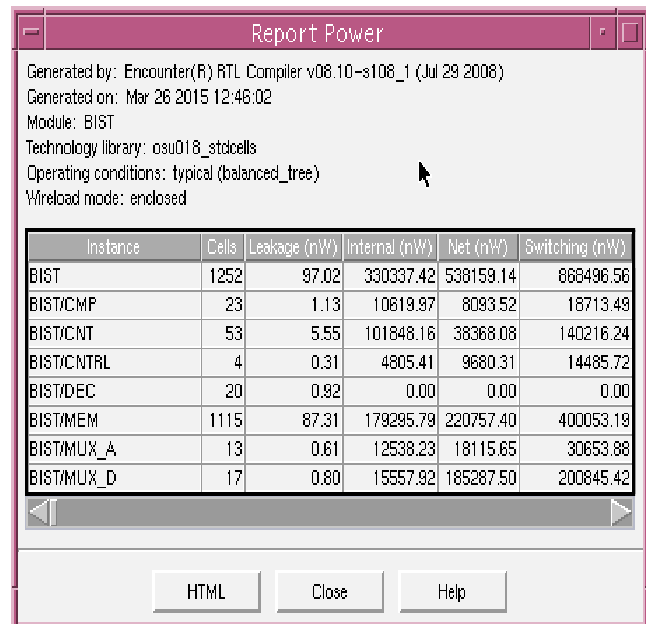
Figure 5. Power Report of Existing Method[5].



Report Power

Generated by: Encounter(R) RTL Compiler v08.10-s108_1 (Jul 29 2008)
Generated on: Mar 26 2015 12:46:02
Module: BIST
Technology library: osu018_stdcells
Operating conditions: typical (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
BIST	1252	97.02	330337.42	538159.14	868496.56
BIST/CMP	23	1.13	10619.97	8093.52	18713.49
BIST/CNT	53	5.55	101848.16	38368.08	140216.24
BIST/CNTRL	4	0.31	4805.41	9680.31	14485.72
BIST/DEC	20	0.92	0.00	0.00	0.00
BIST/MEM	1115	87.31	179295.79	220757.40	400053.19
BIST/MUX_A	13	0.61	12538.23	18115.65	30653.88
BIST/MUX_D	17	0.80	15557.92	185287.50	200845.42

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Figure 6. Power Report of Proposed Design.

Table 1. Comparison of power consumption

MBIST	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (mW)
Existing Method[5]	1258	96.42	350910.96	569433.24	0.9203
Proposed	1252	97.02	330337.42	538159.14	0.8684

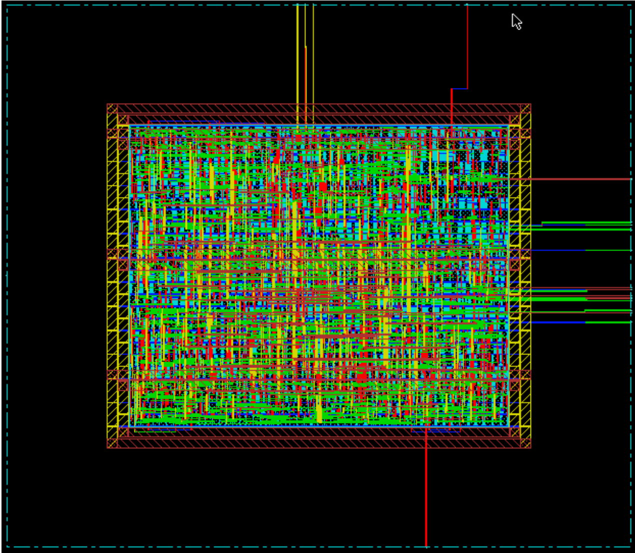

Figure 7. Layout of Proposed MBIST Design.

Proposed BIST architecture also been implemented in Cadence SoC Encounter for layout design and up to GDS-II file generation. Figure 7 shows the layout of the BIST with proposed address generator embedded in it.

5. Conclusion

Through this work, we have attempted to introduce new architecture for address generator which occupies major part of power consumption during testing. The proposed address generator resulted in 5.63% cut-down of switching activity when employed in MBIST. We have also implemented the designed address generator in MBIST architecture which also resulted in reduced power consumption and area occupied as decrease in number of cells is observed from 1258 to 1252. 5.86% and 5.49% of reduction internal and net power consumption is resulted by this architecture. There by employing this low power BIST architectures on-chip can taste low power during test application.

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