

# VLSI Implementation of Telemonitoring System for High Risk Cardiac Patients

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## Abstract

This paper aims in design and development of low cost, light weight, portable Telecardiac system for remote monitoring of cardiac patients. The proposed system employs a Field Programmable Gate Array (FPGA), a reconfigurable platform that performs online analysis of the acquired ECG signal continuously. FPGA based Arrhythmia detector, implemented on a DE2 Altera Cyclone II board is interfaced with GSM/GPS module to alert the physician on a mobile phone about the imminent fatal condition and location of the patient. If the portable system detects any arrhythmia, it automatically sends an alarm condition to the patient's care taker and ambulance centre by sending an SMS that has information about the abnormal condition and location of the patient.

**Keywords:** CVD, FPGA, GSM, GPS, SMS, Telecardiac System, Telemedicine

## 1. Introduction

Nearly 20 million people die each year due to cardiovascular diseases and 22 million people are at risk of sudden failure at any moment. According to a study<sup>1</sup> in UK, it is seen that among patient above 55 years old, who die from cardiac arrest, about 91% die outside hospital, due to a lack of immediate treatment. In case of acute myocardial infarction the survival is related to the “call to needle” time, which should be less than 60 minutes<sup>2</sup>. Patients, who have survived cardiac arrest, ventricular tachycardia or cardiac syncope, face an increased risk of sudden cardiac death. These patients with heart rhythm irregularities (arrhythmia) require some type of monitoring and it is a major part of many healthcare services. It can bring down the need for hospitalization. Today, the conventional method of monitoring a patient discharged from hospital is by using portable Holter monitor and in an emergency situation by using ambulatory ECG recording equipment. However these devices only record a serious rhythm irregularity or transmit the ECG recording to

a hospital server, where the doctor has to go and make the analysis and then initiate a treatment. This is patently time consuming. Early detection and defibrillation is critical for survival.

A cost effective and alternate method for face-to-face consultation is telemedicine or telehealth or e-health which includes diagnosis, consultation and supervision and treat remote patients. The emergence of new technologies in wireless and mobile telecommunication networks, combined with the simultaneous rapid advances in information technology, is leading to many new solutions in the field of telemedicine<sup>3</sup>. Mobile cellular networks like GSM, GPRS and 3G mobile communication aid wireless telemedicine, thereby freeing the doctor and the patient from fixed locations with the added advantage of low cost. These systems facilitate mobility for doctors with 24/7 monitoring capability regardless of physical locations of Physicians/Infrastructure, affordability of the patients for effective and efficient treatment.

In earlier methods, Public switched telephone Networks (PSTN) was employed to implement telemedicine

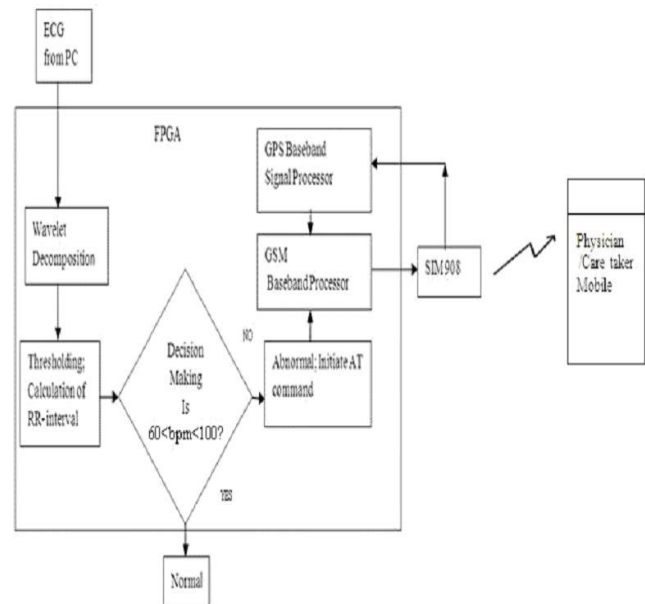
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system. Wireless Access Protocol (WAP) based telemedicine system, Wireless LAN and PDA based physiological monitoring system<sup>4,5</sup>, Bluetooth based ECG monitoring device<sup>6</sup> were implemented in which patient's biosignals were transmitted to a remote central management unit and no online analysis was performed. The criticality of a cardiac patient was analyzed using FPGA based smart diagnostic system<sup>7</sup> but no wireless transceiver was interfaced with the system. A microcontroller based portable system<sup>8</sup> capable of transmitting ECG signal to a remote PC for analysis was implemented by Mitra et al. A mobile Telecardiac system<sup>9</sup> with GPRS transceiver was proposed and simulated in MATLAB environment. ECG signal analysis was performed using ARM microcontroller<sup>9,10</sup>. Many proposals have been made for the analysis of biomedical data using FPGA. FIR filter design for removal of noise using FPGA was discussed by Nian<sup>11</sup>. ECG feature extraction by Weichu et al.<sup>12</sup>, Arrhythmia classification by Mohammad et al.<sup>13</sup>, QRS detection system by Shukl et al.<sup>14</sup>, based on FPGA have been discussed. Praksh et al.<sup>15</sup> developed a real time monitoring system for ECG signal using PIC Microcontroller. However no literature is available for transmission of the critical condition of the patient after the patient side analysis of ECG signal.

Hence the proposed system consists of a FPGA based Arrhythmia detector which is implemented on a DE2 Altera Cyclone II board interfaced with GSM/GPS module to alert the physician on a mobile phone about the imminent fatal condition and location of the patient. If the portable system detects any arrhythmia, it automatically sends an alarm condition to the patient's care taker and ambulance centre by sending an SMS, which has information about the abnormal condition and location of the patient. The main advantage of the proposed system is that real time analysis is performed and does not involve store and forward method.

## 2. Proposed System

The proposed system as shown in Figure 1. consists of a Field Programmable gate array that performs ECG analysis using Integer Wavelet decomposition followed by thresholding technique. Decision whether the person is normal or abnormal is based on calculating the value R-R interval and beat per minute and if any abnormality is detected, the system initiates an AT command to the



**Figure 1.** Proposed Telecardiac System.

inbuilt GSM Baseband Processor module, which sends a SMS to physician or caretaker mobile through the module SIM 908. The proposed system also integrates a GPS Baseband Signal Processor, which performs Acquisition, Tracking and Data processing of the signal received from SIM 908. Therefore; the location of the patient can be continuously monitored. Hence under abnormal condition, the location of the patient is also transmitted for rescue through GSM and SIM 908. FPGA well suits for implementing the Telecardiac system because as arrhythmia detector performs real time analysis, GSM baseband processor has to establish connectivity in the network and at the same time GPS Baseband processor has to process the NMEI data received from SIM 908.

## 3. FPGA based Arrhythmia Detector

The heart of the proposed Telecardiac System (TCS) is the Arrhythmia detector implemented in a Field programmable Gate Array (FPGA). FPGA is preferred in the design of real time operations as it can implement a wide range of logic functions; reconfiguration is possible during runtime; and it provides parallel computing environment. Analysis of the ECG signal is done by performing wavelet decomposition followed by thresholding and decision making.

### 3.1 Integer Wavelet Decomposition

Fiducial points in an ECG signal can be easily determined by wavelet transforms. There are two types of wavelet transforms - continuous wavelet and discrete wavelet transforms. Continuous wavelet is not suitable for biosignal analysis because it provides redundant information. So, Discrete Wavelet Transform (DWT) is preferred in feature extraction from a non stationary signal like ECG. The amplitude range of ECG signal is 1-10mV and its frequency range is 0.05 -100 Hz. Most of the energy content of QRS complex lies in the frequency range of 3 – 40 Hz. So, wavelet decomposition is employed to extract the required QRS complex and to detect any abnormality in the acquired ECG signal. Simulation performed in MATLAB environment using the command “wavedec” shows that 4 level of wavelet decomposition produces a clear QRS complex devoid of noise as shown in Figure 2. Hence, the additional feature in wavelet decomposition is that it does not require filtering circuits in the preprocessing stage.

Hardware implementation of wavelet decomposition is obtained by allowing the ECG signal to pass through low pass filter with transfer function  $g(n)$  and high pass filter with transfer function  $h(n)$  followed by decimation by a factor of 2 as shown in Figure 3.

The logic expression used to obtain Detailed coefficients (D) and Approximation coefficients (A) of the first level by using Integer Wavelet Transform<sup>9</sup> is given below:

$$A1 = \frac{1}{2}x(2n) + \frac{1}{2}x(2n + 1) \tag{1}$$

$$D1 = x(2n) - x(2n + 1) \tag{2}$$

The Approximation coefficients are obtained by using an adder and division is achieved by shifting the bits by

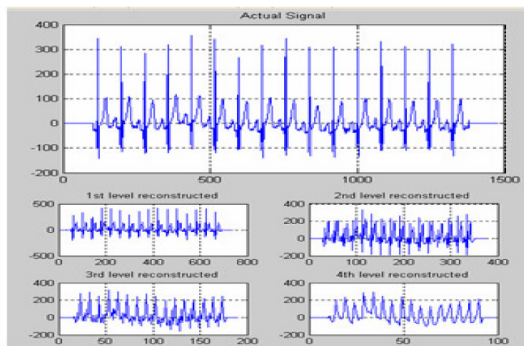


Figure 2. Matlab Simulation.

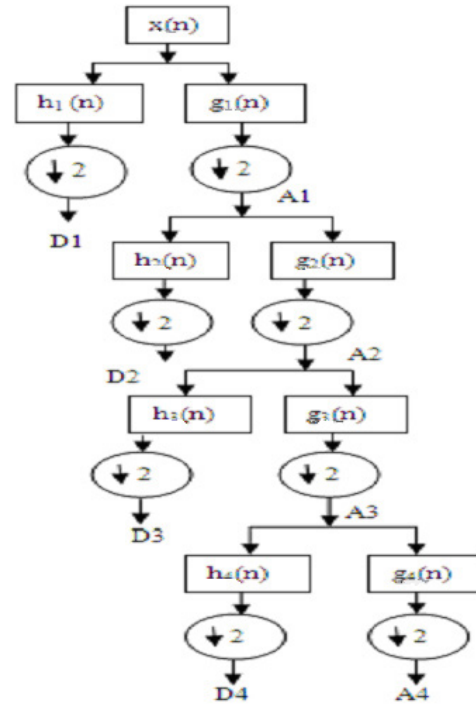


Figure 3. Four level Wavelet Decomposition.

one position. Detailed coefficients (D) are obtained by using a subtractor.

### 3.2 Thresholding and Decision Making

The decomposed signal at the fourth level is used for further processing to determine the R-wave. Hard thresholding technique is employed in which the coefficients below the threshold value are made zero. The first ten coefficients are examined and threshold is fixed to the maximum value.

Threshold = Max (D4),  $i = 1$  to 10. As the new coefficient arrives, threshold value gets updated and this updation is proceeded upto 50 coefficients. For the next set of 50 coefficients, the above steps are followed. An pulse is generated for every non-zero coefficient (from  $i = 1$  to 50) which represents the onset of R-wave. The time at which the first pulse generated is stored as R\_TIME\_1 and the consecutive pulse arrival time is stored as R\_TIME\_2. The difference between R\_TIME\_1 and R\_TIME\_2 represents the R-R interval. The proposed FPGA based arrhythmia detector is functionally verified by using the digitized data from MIT-BIH database and simulation result is shown in Figure 4.

From Figure 3, the R-R interval obtained from Modelsim simulation is 0.98s. Heart rate can be calcu-

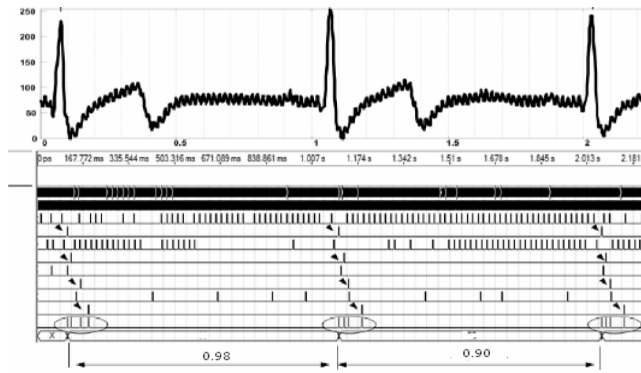


Figure 4. Modelsim simulation.

lated using the formula: Heart rate = 60/R-R interval in seconds; = 60/0.98 = 61 beats per minute. Beat per minute is calculated and the decision making logic circuit in FPGA decides whether the person is normal or abnormal.

## 4. Hardware Implementation and Results

FPGA architecture of the implemented hardware is shown in Figure 5. Arrhythmia detector discussed in section 3 is implemented using Altera DE2 board which contains Altera Cyclone II 2C35 FPGA device; Altera serial configuration device EPCS16; onboard USB blaster for programming; 512kbyte of SRAM; 8 Mbytes of SDRAM; 4Mbytes of flash Memory and RS-232 Transceiver.

The communication between the host computer and the DE2 board is achieved using Altera USB Blaster Driver software. Philips ISP1362 USB controller provides an interface between the host and the device. Configuration data for the cyclone -II FPGA is stored in E<sup>2</sup>PROM chip on DE2 board. Each time power is applied to the board, the configuration data gets automatically loaded from E<sup>2</sup>PROM into FPGA. User programming can be downloaded into FPGA by two methods – JTAG programming (Joint Test Action Group) and Active Serial Programming (AS). The disadvantage of JTAG programming is that configuration is lost when the power is turned off whereas in AS programming, the information can be retrieved even when the power supply to the DE2 is turned off. EPCS16, the on board configuration device loads the data into Cyclone II FPGA. Hence, AS programming is used for programming the FPGA.

TCS now at a prototype stage has been tested and verified with ECG signal from MIT -BIH database and calculation of RR interval has been performed using thresholding technique and interfaced with SIM 900.

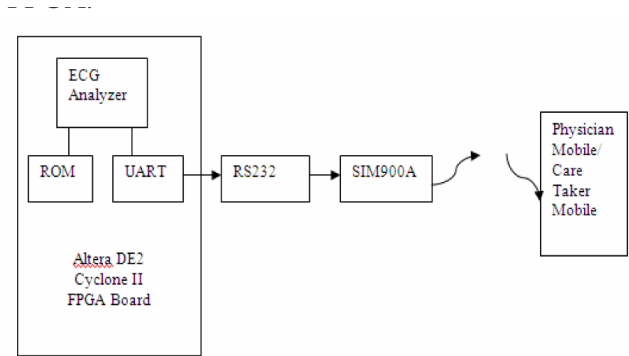


Figure 5. FPGA Architecture with External interface.

Table 1. Output Obtained for various MIT/BIH records

Database - Record Number	Result obtained
300	Abnormal
301	Abnormal
302	Abnormal
303	MI Detected
304	Abnormal
305	Abnormal
306	Abnormal
307	Abnormal
308	Abnormal
309	Abnormal
310	Abnormal
16265	Normal
16272	Normal
16420	Normal
16773	Normal
16539	Normal
16786	Normal
18184	Normal
16483	Normal
106	Abnormal
108	MI Detected
111	MI Detected
112	MI Detected
205	Abnormal
800	Abnormal

The system was designed in Altera's Quartus software and targeted on Cyclone. All blocks were designed using Verilog Hardware Description Language (HDL). As discussed in the previous section and as shown in Figure 5., built-in ECG Analyzer in FPGA calculates beat per minute (bpm). The phone number and the calculated information about the ECG signal are stored in the on-chip memory (Configurable ROM) of FPGA. For normal



person, bpm ranges between 60 and 100. Decision making circuit declares a panic situation if bpm is not in the normal range and automatically sends an AT command to SIM 900A through UART.

SIM 900A is a compact Dual band GSM/GPRS module that can deliver voice, data, and fax. The default baud rate is 9600 with 8-N-1. This module contains a SIM card holder to plug in a valid SIM card for the purpose of accessing the GSM network. The power supply to the GSM modem is +4.1 V, which is obtained by LM7805 voltage regulator. It has LED display to indicate the status of the GSM module like power on, Network access and registration, GPRS connectivity etc. Once the board is powered ON and if valid SIM card is available the corresponding LED will blink in step of 3 second which indicates that GSM modem has registered its connectivity in the network and ready for the application.

Figure 6 shows the prototype of the remote cardiac patient monitoring and alerting system and Figure 7



**Figure 6.** Hardware Implementation of TCS.



**Figure 7.** Mobile phone with Data received from the TCS.

shows the alerting SMS message received in the mobile phone.

## 5. Conclusion

Thus the implemented work can be extended to design a portable system with real time acquisition and processing of ECG signals on the patient side and alarm the doctor or caretaker about the condition of the patient and also a GPS can be incorporated to send the location of the patient, so that recovery of the patient can be done within the crucial hour. At present, work is going on for fabricating a low cost, light weight, portable system on a single FPGA board with multicore platform.

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