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A simple methodology for sinusoidal oscillator design based on simulation of differential equation using AD844 configured as second-generation current conveyor

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Abstract
The work presented in the paper develops a methodology for the design of sinusoidal oscillator based on simulation of differential equation using second generation current conveyors. A practical circuit using the IC AD844 configured as current conveyor (CCII+) with CMOS analog switch DG201 illustrates the methodology. Experimental results are given. The scheme is suitable for frequencies below 1MH$_Z$.

Keywords: Current conveyor, IC AD844, sinusoidal waveform generation, RC oscillator.

Introduction

Generation of sinusoidal function is a common problem encountered by circuit designers (Singh, 1980). Sinusoidal signal generators are required in a number of diverse areas including audio testing, calibration equipment, transducer drives, power conditioning and automatic test equipment (ATE). Control of frequency, amplitude or distortion level is often required and all three parameters must be simultaneously controlled in many applications. A number of techniques utilizing both analog and digital approaches are available for a variety of applications. Each individual circuit approach has inherent strength and weakness, which must be matched against any given applications. Among the methods used for generating sinusoidal waveform, the method used to simulate second order differential equation has received almost no attention. In this paper, a simple design methodology for the realization of stable sinusoidal function over a wide dynamic range based on the simulation of second order differential equation using second generation current conveyor is described, analyzed and studied experimentally.

Methodology and design

The design methodology is simple, straight and offers quality sinusoidal waveform over a range of frequency.

The sinusoidal waveforms with a peak amplitude E and angular frequency ω as described by:

$$V = E.\cos\omega.t \qquad (1)$$

or

$$V = E.\sin\omega.t \qquad (2)$$

are the solution of second order differential equation of the form

$$\frac{d^2V}{dt^2} + \omega^2 V = 0 \qquad (3)$$

with the initial condition imposed. For e.g., eq. (1) is the solution of equation (3) provided

$$\left.\begin{aligned} \left.\frac{dV}{dt}\right|_{t=0} &= 0 \\ \text{and} \\ V\big|_{t=0} &= E \end{aligned}\right\} \qquad (4)$$

Similarly, eq. (2) is the solution of eq. (3) provided

$$\left.\begin{aligned} \left.\frac{dV}{dt}\right|_{t=0} &= \omega E \\ \text{and} \\ V\big|_{t=0} &= 0 \end{aligned}\right\} \qquad (5)$$

In principle, the eq. 3 can be implemented as illustrated (Fig. 1) to provide sinusoidal output waveforms under different sets of initial conditions as documented in eq. 4 and eq.5. The implementation of the initial conditions in eq. 4 is easy and straight forward compared to that documented in eq. 5 as the initial conditions attached with eq. 5 are frequency dependent. This suggests that circuit implementation of eq. 3 with eq. 4 which yields sinusoidal waveform as in eq. 1 is somewhat easy and deserves further investigations.

The voltage mode operational amplifiers (op amp) configured as an integrator (Fig. 2) may be used to implement the scheme as depicted in (Fig.1). However, the integrator as shown in (Fig. 2) poses a problem in applying the initial condition as the capacitor is floating. Moreover, floating capacitor is not preferred in IC design methodology. In recent past second generation current conveyor (CCII), because of its attractive features, has been widely used in circuit design (Wilson, 1990; Sedra *et al.*, 1990; Toumazou *et al.,* 1990). It is now well known that IC AD844 from analog devices implements the features of positive second generation current conveyor (CCII+) with an additional unity gain voltage amplifier (Svoboda *et al.,* 1991). The circuit symbol of AD844 (Khan Anwar *et al.*, 2002; Khan Anwar *et al.*, 2005)

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Fig. 1. Scheme for implementation of second order differential equation with no damping

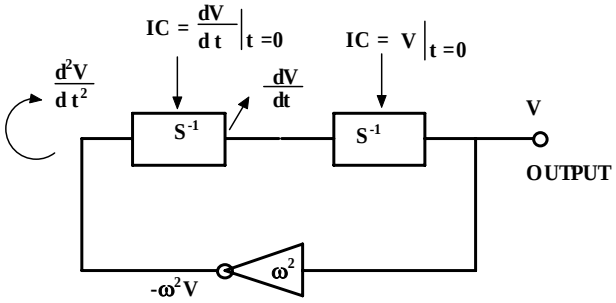


Fig. 2. A typical op amp based integrator

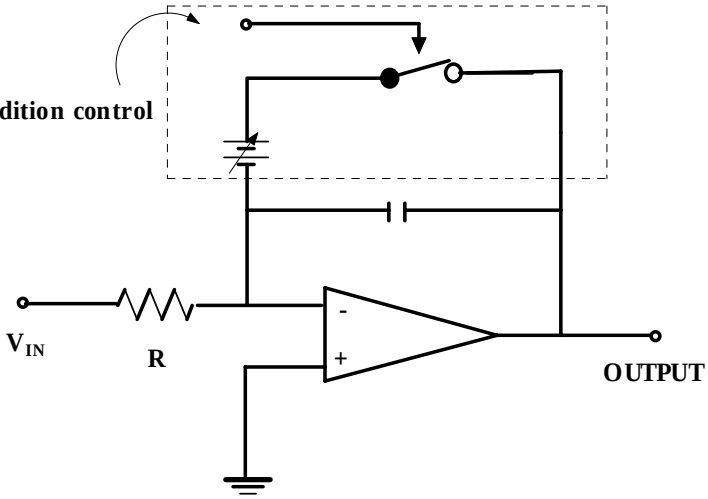


Fig. 3. Equivalent circuit symbol of IC AD844

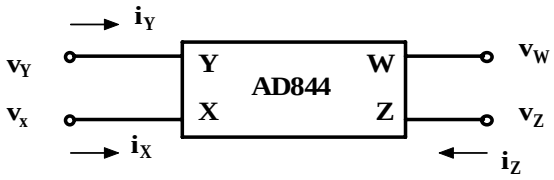


Fig. 4. AD844 based integrator
(a). Positive integrator
(b). Negative integrator

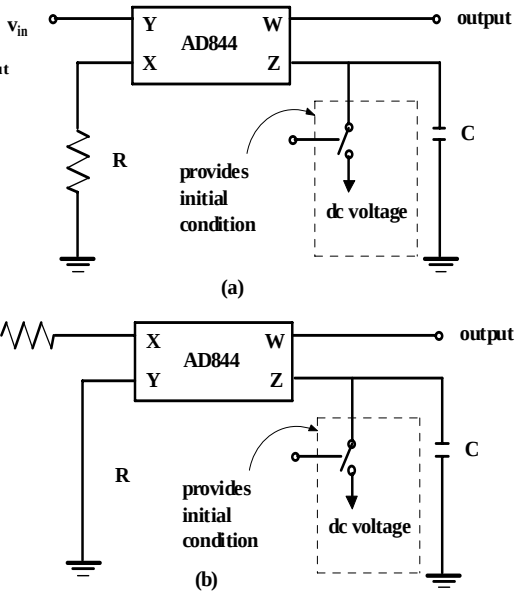


Fig. 5. Proposed current conveyor (AD844) based scheme for the generation of sinusoidal wave form

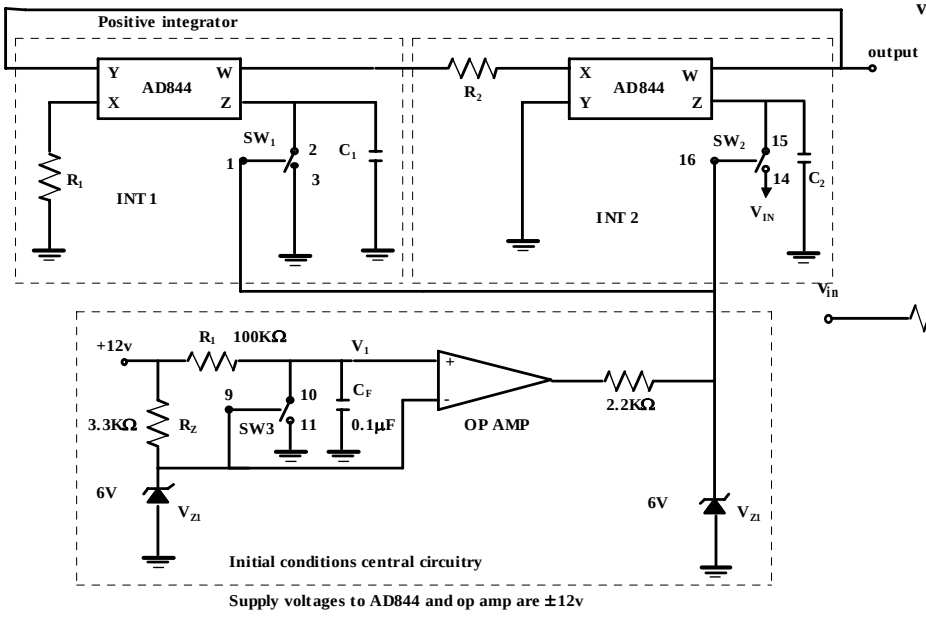
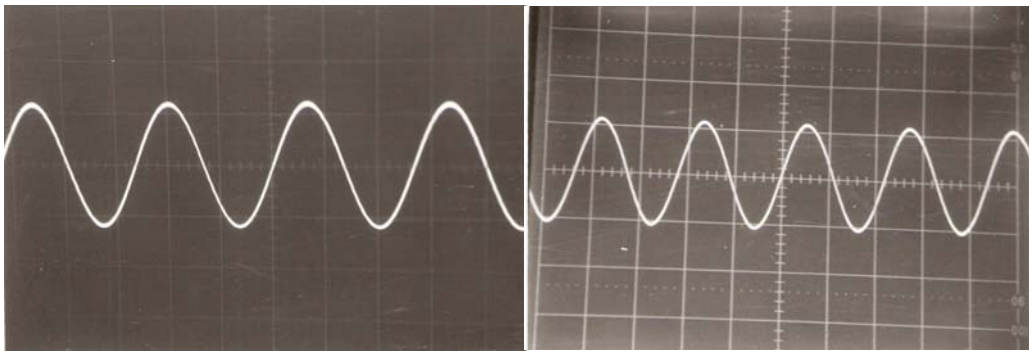


Fig.6. Oscillograms showing the oscillations at frequencies 8 KHz & 227 KHz respectively.



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embodying the features of CCII+ is shown in (Fig. 3) whose terminal characteristics are written as:

$$\left.\begin{aligned} i_y &= 0 \\ v_x &= v_y \\ i_z &= i_x \\ v_w &= v_z \end{aligned}\right\} \qquad (6)$$

The current at terminal Z thus depends only on the input current i_x at terminal X which may be injected directly at X, or it may be produced by the copy of the input voltage v_y, from terminal Y, acting across the impedance connected at X. The voltage v_w at W tracks the voltage v_z at terminal Z. By convention, positive is taken to mean i_x and i_z both flowing simultaneously towards or away from the conveyor (Fig. 3). An integrator circuit employing current feedback amplifier (Mahattanakul & Toumazou, 1996) and current conveyors (Makris &Toumazou, 1990; Nandi & Ray, 1993) have been proposed. An integrator circuit implemented with AD844 (Fig. 3) with the grounded capacitor is depicted (Fig. 4) wherein the circuitry used to enforce the initial condition does not pose problem to IC circuit designers.

The proposed scheme of generating sinusoidal oscillations using AD844 configured as the positive second generation current conveyor (CCII+) with a unity gain voltage amplifier (buffer) is shown in Fig. 5. The circuit built around IC AD844 marked as 'INT 1' as shown under the dotted lines box is a positive integrator with a time constant $R_1 C_1$ followed by a negative integrator with time constant $R_2 C_2$ built around AD844 marked as ' INT 2'. The switches placed across C_1, C_2 and C_F are obtained from CMOS quad SPST analog switches DG201 with the pin numbers as depicted in the Fig. 5. The op amp is configured as voltage comparator and provides a dc output voltage to the control pins of DG201 sufficient enough to operate the switches as per the truth table (Table 1).

The circuit shown in Fig. 5 operates as follows:
Before the power is switched ON, switches SW_1, SW_2 and SW_3 are all in ON position (Table 1). However, immediately after the power is switched on, short circuit across C_F is lifted (Table 1) and voltage V_F across C_F starts increasing exponentially with time constant of $R_F C_F$. During this interval, however, switches SW1 and SW2 are closed giving V_{C1} = 0V (initial condition, i.e. $\left(dV/dt\right)_{t=0}$ and $V_{C2} = V_{Z1}$ (initial condition, i.e. $V\big|_{t=0} = V_{Z1}$) . When V_F exceeds V_{Z1}, output of the op amp switches to positive high giving signal to SW_1 and SW_2 to open. At this stage, the two integrators start functioning and output cosine waveform is generated with the peak amplitude of V_{Z1} (initial condition put on C_2) and the frequency of oscillations ω is given by:

Table1. Truth table for CMOS analog switch DG201

Logic	DG201
0	ON
1	OFF

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \qquad (7)$$

The circuit shown in Fig. 5 was implemented in the laboratory with IC AD844 from analog devices and CMOS analog switches DG201. The resistors and capacitors used in the circuit were accurate to ±5% and ±10 %, respectively. The oscillograms at frequencies 8 KH_Z and 227 KH_Z are shown in (Fig. 6) respectively. Note that the peak amplitude can be varied by V_{Z1} using a simple voltage divider across zener diode and the frequency of oscillations is controlled either by R (R_1 or R_2) or C (C_1 or C_2). The scheme is suitable for frequencies below 1 MH_Z. The frequency range could be extended using high frequency analog switches (Premont & Abouchi, 1998).

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